Plasma Science and Technology Division
Room B131 - Session PS+EM-TuM

Advanced FEOL

Moderator: Alok Ranjan, TEL Technology Center, America, LLC

8:00am **PS+EM-TuM1 Investigation on Plasma Etch Technology Enabling Si/SiGe MOSFET Process Integration**, ***Yohei Ishii***, Hitachi High Technologies America Inc.; *Y.-J. Lee, W.-F. Wu,* Taiwan Semiconductor Research Institute, Taiwan, Republic of China; *R. Sugano,* Hitachi, Ltd., Japan; *K. Maeda,* Hitachi High Technologies America Inc.; *H. Ishimura,* Hitachi High-Technologies Taiwan Corp., Taiwan, Republic of China; *M. Miura,* Hitachi High Technologies, Japan **INVITED**

Many challenges have emerged due to down-scaling of device structure in order to follow Moore's law. By modifying the transistor structure from planar to Fin-type Field Effect transistors (FinFETs), transistor electro-statics were improved, which led to overcoming short-channel effects. However, the change is no longer sufficient, and the semiconductor industry faces difficulty to further improve the transistor performance. One of the promising candidates for the improvement in sub-10nm process is to utilize Silicon/Silicon-germanium (Si/SiGe) dual channel FinFETs (Si in n-FETs and SiGe in p-FETs). In this case, simultaneous etching of Si and SiGe is required [1]. However, etch rate of SiGe is greater than Si for halogen chemistries commonly used in Si etch. Therefore, it is required to develop selective Si etch over SiGe for etch rate control between these two materials.

In order to maximize electrical performance of SiGe, modifying the SiGe surface composition into Si-rich surface at SiGe/gate-oxide interface is critical to reduce interface state density due to the impact on sub-threshold characteristics [2]. Traditional methods to produce Si-rich surface are epitaxial growth of Si cap over SiGe fin [3] and GeOx-scavenging process [4]. However, thermal budgets of these methods are relatively high, and there are concerns of strain relaxation in SiGe channel and Ge diffusion into Si substrate, both of which deteriorate the FET characteristics. Hence, a low-temperature process to produce Si-rich surface is required.

In this presentation, we will present two phenomena; one is Si-SiGe selective etch control, and the other is SiGe surface composition modification of SiGe into Si-rich surface by low temperature plasma. We will first present a plasma process, which etches Si selective to SiGe for Si-SiGe etching control, and will discuss the etching mechanism of the selective etching. We will then present the composition modification into Si-rich surface by utilizing Si segregation from the low temperature plasma process. This plasma etch technique can solve the etch rate control and surface composition challenges, which can be a promising scheme for realizing well-controlled SiGe finFETs with improved characteristics.

[1]. Y. Ishii et. al., Jpn. J. Appl. Phys. **57**, 06JC04 (2018).

[2]. C. H. Lee et. al., IEDM Tech. Dig., p.31.1.1., 2016

[3]. H. Mertens, et al., VLSI Tech. Dig., p.58, 2014

[4] C.H. Lee, et. al., VLSI Tech. Dig., p. 36, 2016

8:40am **PS+EM-TuM3 Etching of Sub-10 nm Half-pitch High Chi Block Copolymers for Directed Self-Assembly (DSA) Application**, ***Maria Gabriela Gusmão Cacho***, *P. Pimenta-Barros, K. Benotmane, A. Gharbi, M. Argoud,* CEA-LETI, France; *C. Navarro,* Arkema France, France; *K. Sakavuyi,* Brewer Science Inc.; *R. Tiron, N. Possémé, S. Barnola,* CEA-LETI, France

As the semiconductor industry approaches the smaller technologic nodes such as the sub-10 nm, conventional lithography technologies have reached their limit. Among the different approaches investigated to continue pattern scaling, Directed Self-Assembly (DSA) of Block Copolymers (BCP) is one of the most promising due to its simplicity, low manufacturing cost and capability to design high density cylindrical or line/space patterns. For the last few years, PS-*b*-PMMA has been the most used BCP for this application. However, since the minimum feature size for the PS-*b*-PMMA system is limited to ~13 nm due to its low interaction parameter (also known as "chi"), new systems have been developed to achieve higher resolution by improving its microphase separation strength, thus obtaining the so called "high chi" BCPs.

In this paper, the high chi BCP system investigated is a modified PS-*b*-PMMA that presents a pitch of 18 nm, which will be referred to as "L18". One critical step for its integration is the PMMA removal selectively to the PS. The results obtained with both dry and wet etching of the L18 BCP are presented, highlighting the challenges encountered due to its smaller dimensions.

A wet PMMA removal process based on UV exposure followed by IPA rinse will be presented. An Ar/O_2 dry etch step for the brush layer opening was developed and the transfer of the line/space pattern into the SiO_2 and Si underlayers was demonstrated for the L18 BCP. However, this wet development is expected to cause pattern collapse when the BCP will be guided by chemoepitaxy due to capillary forces.

Therefore a complete PMMA removal by dry etching alone was also investigated. Different etching chemistries based on $CH_3F/Ar/SO_2$, CH_4/N_2 or cyclic CO + CO/H_2 were applied to the modified PS-*b*-PMMA BCPs with a 30 nm pitch and with an 18nm pitch (L18). For the 30 nm-pitch BCP, all three plasma chemistries allow the complete PMMA and brush layer removal by dry etching and the subsequent pattern transfer into the SiO_2 layer. In contrary, for the L18 BCP, the $CH_3F/Ar/SO_2$ plasma does not present enough PS budget for pattern transfer due to its low selectivity and the small thickness of the BCP. For the more passivating chemistries such as CH_4/N_2 and cyclic CO + CO/H_2, which have higher selectivity, we observe the formation of bridges that prevent complete pattern transfer. We used *ex-situ* X-ray Photoelectron Spectroscopy (XPS) to investigate the origin of these bridges and to understand the etching mechanisms present.

9:00am **PS+EM-TuM4 Mechanism of Highly Selective SiCN Etchings Using NF_3/Ar-based Gases**, ***Miyako Matsui***, Hitachi Ltd., Japan; *K. Kuwahara,* Hitachi High-Technologies Corp., Japan

Highly selective etchings over various other materials are increasingly required to achieve self-aligned processes, which provide higher density devices without shrinkage of the pattern dimensions in three-dimensional devices, such as fin-based field-effect transistors. In a self-aligned process, SiCN etching is required to achieve high selectivity to both SiO_2 and Si_3N_4. However, it had been difficult to achieve high selectivities to both SiO_2 and Si_3N_4 using fluorocarbon gas chemistries. For example, selectivity to SiO_2 increased using a hydrofluorocarbon plasma, while selectivity to Si_3N_4 decreased. So, it is important to investigate gas chemistries to simultaneously control selectivities to various materials.

In this study, mechanisms for highly selective SiCN etchings with microwave ECR plasma using NF_3/Ar-based gases were investigated over various materials. The rate of SiCN etching using NF_3/Ar plasma was higher than that of other materials, which were TiN, poly-Si, SiO_2, and Si_3N_4. The SiCN was etched with NF_3/Ar plasma, which formed SiF_x and FCN. On the other hand, other materials were etched with low rates. To achieve higher selectivities, the effects of adding gases to NF_3/Ar plasma on various materials to inhibit etching were analyzed by X-ray photoelectron spectroscopy (XPS).

Firstly, a highly selective SiCN etching over poly-Si was achieved by adding O_2 to NF_3/Ar plasma. This was because poly-Si etching was inhibited by the formation of a 1.0 nm-thick oxidized layer, which protected the poly-Si surface from the etching reaction with F radicals. The SiCN etch rate also decreased when the poly-Si etching was stopped. However, C atoms contained in the SiCN layer reacted with O radicals and controlled oxidization of the SiCN surface.

Next, highly selective SiCN etchings over SiO_2 and Si_3N_4 were achieved by using a NF_3/Ar-based plasma by which deposited layers were formed on the surfaces. The deposited layers formed on the SiO_2 and Si_3N_4 protected the surfaces from being etched by reacting with F radicals. On the other hand, the deposited layer was thought to be more difficult to be formed on the SiCN.

Lastly, highly selective etching over TiN was achieved by using H_2-added plasma. XPS result showed that a thin protective layer containing TiF_x and ammonium fluoride, which is decomposed over 673K, had been formed on the TiN surface. The protective layer formed on the TiN surface was very effective at protecting the TiN from being etched by F radicals.

In conclusion, we achieved extremely highly selective SiCN etchings over various materials by forming protective layers, which were formed on non-etched materials by adding gases to NF_3/Ar plasma.

9:20am **PS+EM-TuM5 Impact of Plasma Process on Source/Drain Epitaxy Film**, ***Yun Han***, *B. Messer, M. Sapel, H. Kim, Y. Shi, M. Wang, Y. Trickett, K. Maekawa,* TEL Technology Center, America, LLC; *K. Taniguchi, S. Morikita,* Tokyo Electron Miyagi Ltd., Japan; *A. Metz, P. Biolsi,* TEL Technology Center, America, LLC

Middle-of-Line (MOL) contact open by plasma etching is a very critical step in logic IC fabrication. Source/Drain Epitaxy (S/D Epi) film as a key element in device transistors controls device performance in various aspects. S/D

Epi film damage induced by plasma etch processes have been one of the challenges in MOL integration. Epi film damage includes surface roughening and oxidation, crystal structure relaxation and elemental doping, all of which could lead to uncontrolled variation and degradation in electrical performance of the devices. In this paper, SiGe (known pMOS S/D material) film damage post varying CCP plasma conditions have been studied by utilizing different characterization techniques including X-ray photoelectron spectroscopy (XPS), Transmission Electron Microscope (TEM) / Energy-dispersive X-ray spectroscopy (EDS), Rutherford backscattering spectrometry (RBS) and Secondary ion mass spectroscopy (SIMS). Various CCP plasma conditions include changes in gas chemistries (N/H/O/C/F/Ar), plasma source/bias power and chamber configurations. Electrical response on short loop device wafers have been collected and correlated with observed physical/chemical changes in S/D Epi film post plasma processes. We also performed molecular dynamics, quantum chemistry and chamber scale simulation to understand the fundamental chemical behavior and characterize the surface/chemical properties between provided plasma and SiGe film at various ion energy and ion/radical flux in an atomic/molecular level. The study provides a comprehensive understanding in plasma damage to S/D Epi film and a fundamental guideline in optimizing plasma processes to achieve ideal contact open etch with minimal damage on source/drain Epi film.

9:40am **PS+EM-TuM6 CCP Dry Clean Process Development Using Quadrupole Mass Spectrometer and Optical Emission Spectroscopy**, ***Harutyun Melikyan***, *A.D. Martinez, S.C. Pandey, M. Koltonski, G. Sandhu,* Micron Technology

Dual frequency capacitive coupled plasmas provide flexible control of ion energy distributions, enabling high selectivity for etching of different materials, and flexibility to develop more efficient dry clean processes for higher productivity. It is common for each patterned wafer etch to have pre and post dry clean steps, with and without wafer, respectively. The primary focus of dry etch engineers is to design high etch rate processes, with minimized process time, and without changing the critical dimensions. Additionally, significant gains can be achieved by optimizing the dry clean recipes because they contribute significantly to the raw process time. In some cases, it can take a long time to achieve proper pre and post conditioning of the chamber.

In this work, we show that real-time monitoring techniques can be used to provide insight into the etch process byproducts, enabling intelligent development of the dry clean recipes. Integrating quadrupole mass spectrometry and optical emission spectroscopy with the capacitive coupled plasma reactor, and monitoring in parallel, we were able to identify 99% of the patterned wafer etch byproduct species with high confidence. Knowing the etch byproducts provides a clear path to an optimized dry clean process. We were then able to develop the dry clean recipe with appropriate precursor gases to increase volatile byproducts significantly (e.g. SiF4 at 33%) and minimize non-volatile byproducts (e.g. ammonium salts at <1%), resulting in a 70% reduction of dry clean process time.

11:00am **PS+EM-TuM10 Surface Reaction of Atomic Hydrogen with SiGe Surface Compared with Si Through Ab-initio Calculations**, ***Ryoko Sugano***, Hitachi, Ltd., Japan*; Y. Ishii, K. Maeda,* Hitachi High Technologies America Inc.*; M. Miura, K. Kuwahara,* Hitachi High Technologies, Japan

Simultaneous etching of Si and SiGe is an indispensable process for high throughput in the fabrication of Si/SiGe dual-channel FinFETs. SiGe etch rate is higher than Si etch rate by typical halogen chemistries used for Si etching [1]. Therefore, to control the etch rate between Si and SiGe, it is necessary to develop the chemistry that gives a higher Si etch rate than SiGe etch rate. Recently Ishii et al. have reported that hydrogen plasma selectively etched Si over SiGe, showing the selective Si removal over Ge [2]. In spite of selective Si etching over Ge, the Si-rich surface was observed after the hydrogen plasma exposure. They have attributed the Si-rich surface to hydrogen-induced Si surface segregation [2].

To understand the mechanism of the experimental phenomena on SiGe film described above, we performed ab-initio calculations that combined geometry optimizations and Nudged Elastic Band calculations. In the hydrogen-terminated SiGe surface system, we assumed the reacted states of SiGe were single dimer, in which three hydrogen atoms adsorbed on one of the dimer atoms (SiH3, GeH3) and a single hydrogen atom adsorbed on another of the dimer atoms. We found that the formation with SiH3 was energetically stable and was easy to desorb with a lower activation energy than that with GeH3. We considered that the selective Si removal over Ge was caused by both the selective formation and selective desorption of SiH3. We also calculated the formation energy of the SiGe surface immediately after selective Si removal, which originated from dimer breaking. It was found that the site exchange between the Ge atom in the first layer and the Si atom in the second layer was energetically favorable when another dimer atom left on the surface was terminated with a hydrogen atom. In conclusion, we confirmed experimental results of both selective Si etching over SiGe and Si surface segregation under the condition of hydrogen plasma by performing ab-initio calculations.

[1] G. S. Oehrlein, et al., Appl. Phys. Lett. 58, 2252 (1991).

[2] Y. Ishii et al., Jpn. J. Appl. Phys. 57, 06JC04 (2018).

11:20am **PS+EM-TuM11 Nanopantography with Reusable Membrane-based Electrostatic Lens Arrays**, ***Ryan Sawadichai***, *Y.-M. Chen, P. Basu, V.M. Donnelly, P. Ruchhoeft, D.J. Economou,* University of Houston

Nanopantography is a method for massively parallel writing of nano-sized patterns using an ion beam in combination with a reactive gas. In this process, a broad area, collimated, nearly-monoenergetic ion beam is directed towards an array of micron-scale electrostatic lenses in direct contact with a substrate. By applying an appropriate DC voltage to the lens array with respect to the substrate, the ion beamlet entering each lens converges to a fine spot that can be 100 times smaller than the diameter of each lens. Previously, lenses fabricated directly on the silicon substrate were used to etch 3 nm diameter holes in silicon by exposure to a monoenergetic Ar^+ ion beam and chlorine gas. This work reports on the development of removable and reusable free-standing membrane-based electrostatic lens arrays that are designed to pattern any conducting surface. The lens arrays were fabricated on a silicon wafer coated with PMGI, SU-8, gold, copper, and PMMA. Lens openings were lithographically defined, and an acrylic frame was placed over the array. The lens patterns were etched through the SU-8 and the membrane was released by dissolution of the PMGI layer. The applied voltage used to focus the ion beamlets also served to electrostatically clamp the lens array to a conducting substrate, which was observed as a flattening of the membrane against the substrate surface and an increasing capacitance measured between the lens array and the substrate. An array with lens diameters between 0.8 µm and 1.5 µm and dielectric thickness of 1 µm was used to pattern nanoscale features on a silicon substrate using a 70 eV Ar^+ ion beam and chlorine gas. Ion trajectory simulations were performed to understand the sensitivity of minimum feature size to the variation of lens potential, lens aspect ratio, and lens size. Simulations agreed with the experimentally observed patterns when chromatic and spherical aberrations were considered. With a thinner dielectric and higher lens voltage, it should be possible to print sub 10-nm features in a step and repeat nanopantography process.

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