Electronic Materials and Photonics Division
Room A214 - Session EM+PS+TF-MoA

New Devices and Materials for Logic and Memory

Moderator: Rehan Kapadia, University of Southern California

1:40pm **EM+PS+TF-MoA1 Short-term Plasticity to Long-term Plasticity Transition Mimicked by High Mobility InP FETs with TiO_2 Trapping Layer**, ***Jun Tao***, *R. Kapadia,* University of Southern California

Memory is widely believed to be encoded and stored in the central nervous system by altering the synapse strength via activity-dependent synaptic plasticity between millions of neurons in vertebrates. Consolidations from short-term plasticity (STP) to long-term plasticity (LTP) not only transform the important external stimuli to permanently stored information but release storage space for accepting new coming signals. Although memristor technology (e.g. RRAM) has been reported to mimic the STP and LTP characteristics and exhibited its merit in density comparing to traditional CMOS based SRAM technology, some conventional memristors suffer non-ideal operation speed, small dynamic range, and high resistance variation.

In our work, the single crystal Indium Phosphide (InP) based synaptic devices demonstrated its advantages not only in the emulation of the synaptic functions for both STP and LTP characteristics but also in the controllability of transition from STP to LTP. Since we interpret gate voltage pulses as the pre-synaptic action potentials, the source-drain current as post-synaptic current, and the channel conductance as synaptic weight, the consolidations from STP to LTP are elaborately demonstrated through mediating multiple action potential parameters like pulse numbers, pulse intervals (or rates), and pulse durations. The synaptic devices we demonstrated here are essentially single crystal channel InP Field Effect Transistors (FETs) fabricated on Si/SiO_2 substrates with the templated liquid-phase (TLP) method. In addition, TiO_2 trapping layer is inserted into the gate dielectric layer to provide extra deeper trap states. The 'ratchet' mechanism is utilized to have the charges 'fall' into the TiO_2 well and implement the transition from STP to LTP effectively.

2:00pm **EM+PS+TF-MoA2 Magnetic Domain Wall Devices for Artificial Neural Network**, ***Saima Siddiqui***, *S. Dutta, A. Tang, L. Liu, M. Baldo, C. Ross,* MIT

Magnetic domain wall devices are promising candidates for logic [1] and storage class memory [2]. Due to the non-volatility and energy-efficient switching, this type of device is one of the prime candidates for in memory computing and brain-inspired computing. In-memory computing is a non-von-Neumann architecture where data computation and storage are done locally to reduce the data movement between the processor and the storage memory [3]. The layer-by-layer operations of data require synapses (i.e. variable resistors whose resistance vary linearly with the input) and activation function generators between layers (i.e. variable resistors whose resistance vary non-linearly with the input current).

Domain walls' motion in a magnetic wire is a function of applied current due to spin-orbit torque from an adjacent heavy metal (Fig. 1). The current density and spin orbit torque can be modified along the wire by adjusting the width of the heavy metal. The spin orbit torque then becomes a function of the domain wall position, which makes the domain wall motion a nonlinear function of the applied current (Fig. 2). Linear and nonlinear domain wall motion can be detected via magnetoresistance by using a magnetic tunnel junction in which the magnetic wire forms the free layer. The electrical detection is necessary for the analog matrix multiplication in neuromorphic accelerator. However, domain walls are pinned due to the magnetostatic energy minima on the sides of the MTJ. The synaptic (Fig. 3) and activation function (Fig 4) like magnetoresistive behavior can still be generated by using multiple MTJs in parallel. In this study, we demonstrate linear and nonlinear domain wall motion in magnetic wires and modify the design of magnetic tunnel junctions to convert these motions into magnetoresistance. The experimental observations of the device characteristics agree with both analytical and micromagnetic modeling.

[1] J. A. Currivan-Incorvia, S. Siddiqui, S. Dutta, E. R. Evarts, J. Zhang, D. Bono, C. A. Ross, and M. A. Baldo, Nat Commun., 7, 10275 (2016).

[2] Stuart S. P. Parkin, Masamitsu Hayashi, and Luc Thomas, Science, Vol. 320, Issue 5873, pp. 190-194 (2008)

[3] Jacob Torrejon, Mathieu Riou, Flavio Abreu Araujo, Sumito Tsunegi, Guru Khalsa, Damien Querlioz, Paolo Bortolotti, Vincent Cros, Kay Yakushiji, Akio Fukushima, Hitoshi Kubota, Shinji Yuasa, Mark D. Stiles & Julie Grollier, Nature volume 547, pp. 428–431 (2017).

2:20pm **EM+PS+TF-MoA3 Ferroelectric Devices for Non-von Neumann Computing**, ***Zheng Wang***, *A. Khan,* Georgia Institute of Technology **INVITED**

Excitation and inhibition go hand in hand in neuronal circuits in biological brains. For example, neurons in the visual and the auditory cortices provide excitatory responses to visual and auditory stimuli, respectively. On the other hand, interneurons in the central nervous system provide inhibitory signals to downstream neurons thereby imparting regulation and control in neuronal circuits—the loss of which often causes neurodegenerative disorders. These neuro-biological facts have inspired the bio-mimetic computational perspective that artificial, excitatory neurons need to be paired with inhibitory connections for functional correctness and efficient compute models such as spiking neural networks.

In this talk, we will introduce a ferroelectric neuromorphic transistor platform [1,2] which can (1) efficiently incorporate both excitatory and inhibitory inputs in the simple two transistor topology of an artificial, ferroelectric spiking neuron, and (2) emulate several classes of biological spiking dynamics (such as regular, fast, Thalamo-Cortical spiking and so on). We will discuss the recent experimental demonstrations of ferroelectric spiking neurons. The talk will end with a simulation experiment where a full-scale spiking neural network was implemented using experimentally calibrated ferroelectric circuit models and the network was benchmarked analog CMOS and other emerging device technologies.

References:

[1] Z. Wang, B. Crafton, J. Gomez, R. Xu, A. Luo, Z. Krivokapic, L. Martin, S. Datta, A. Raychowdhury, A. I. Khan, "Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering," *The 64th International Electron Devices Meeting (IEDM 2018)*, 2018.

[2] Z. Wang, S. Khandelwal & A. I. Khan, "Ferroelectric oscillators and their coupled networks," IEEE Electron Dev. Lett. 38, 1614 (2017).

3:00pm **EM+PS+TF-MoA5 Ultrafast Measurement of Nanoseconds Polarization Switching in Ferroelectric Hafnium Zirconium Oxide**, ***Mengwei Si***, *P. Ye,* Purdue University

Ferroelectric (FE) hafnium oxides (HfO_2) such as hafnium zirconium oxide (HZO) is the promising thin film ferroelectric material for non-volatile memory applications. The ultrafast measurements of polarization switching dynamics on ferroelectric (FE) and anti-ferroelectric (AFE) hafnium zirconium oxide (HZO) are studied, with the shortest electrical pulse width down to as low as 100 ps. The transient current during the polarization switching process is probed directly. The switching time is determined to be as fast as 10 ns to reach fully switched polarization with characteristic switching time of 5.4 ns for 15 nm thick FE HZO and 4.5 ns for 15 nm thick AFE HZO by Kolmogorov−Avrami−Ishibashi (KAI) model. The limitation by parasitic effect on capacitor charging is found to be critical in the correct and accurate measurements of intrinsic polarization switching speed of HZO. The work is in close collaborations with Xiao Lyu, Wonil Chung, Pragya R. Shrestha, Jason P. Campbell, Kin P. Cheung, Haiyan Wang, Mike A. Capano and was in part supported by SRC and DARPA.

3:20pm **EM+PS+TF-MoA6 Interfacial Charge Engineering in Ferroelectric-Gated Mott Transistors**, *XG. Chen, Y. Hao, L. Zhang,* ***Xia Hong***, University of Nebraska-Lincoln

Ferroelectric field effect transistors (FeFETs) built upon Mott insulator channel materials have been intensively investigated over the last two decades for developing nonvolatile memory and logic applications with sub-nanometer size scaling limit. However, the intrinsically high carrier density of the Mott channel (10^{22}-10^{23}/cm^3) also imposes significant challenges in achieving substantial modulation of the channel conduction. In this work, we exploit the intricate interplay between interfacial charge screening and transfer effects in epitaxial heterostructures composed of two strongly correlated oxide layers, one layer of rare earth nickelate $R$$NiO_3$ (R = La, Nd, Sm) and one layer of (La,Sr)MnO_3 (LSMO), to realize a giant enhancement of the ferroelectric field effect in Mott-FeFETs with a $Pb(Zr,Ti)O_3$ gate. For devices with 1-5 nm single layer $R$$NiO_3$ channels, the room temperature resistance switching ratio (R_{off}-R_{on})/R_{on} increases with decreasing channel thickness till it reaches the electrical dead layer thickness. For devices built upon $R$$NiO_3$/LSMO bilayer channels, the resistance switching ratio is enhanced by up to two orders of magnitude compared with the single layer channel devices with the same channel thickness. Systematic studies of the layer thickness dependence of the field effect show that the LSMO buffer layer not only tailors the carrier density profile in $R$$NiO_3$ through interfacial charge transfer, but also provides an

extended screening layer that reduces the depolarization effect in the ferroelectric gate. Our study points to an effective strategy for building high density nanoelectronic and spintronic applications via functional complex oxide heterointerfaces.

4:00pm **EM+PS+TF-MoA8 The Interface of Transition Metal Dichalcogenides and Ferroelectric Oxides**, ***Maria Gabriela Sales***, *S. Jaszewski, S. Fields, R. Christopher, N. Shukla, J. Ihlefeld, S. McDonnell,* University of Virginia

Transition metal dichalcogenides (TMDs) are an interesting class of materials because of their unique properties owing to their 2D nature, wherein layers that are covalently bonded in-plane are held together by van der Waals forces in the out-of-plane direction, similar to graphene. However, unlike graphene, semiconducting TMDs have a band gap that is tunable with layer thickness, allowing control over its properties depending on specific applications. One such application is in ferroelectric-based transistors, which have high potential for use in memory and logic, but whose major drawback in integration is the poor semiconductor-ferroelectric interface when using silicon as the semiconducting channel, due to issues such as interdiffusion across the interface. Thus, a promising alternative route is using a TMD as the channel with a ferroelectric material as the gate dielectric. This is expected to have an improved interface quality because of the fact that TMDs have no dangling bonds at the surface and are highly stable in-plane. In this study, we focus on a mixture of hafnium oxide and zirconium oxide as our ferroelectric material, with zirconium stabilizing the ferroelectric phase in hafnia. We explore the TMD/ferroelectric structure, addressing certain integration issues in growth, and looking at their interface chemistry and thermal stability. Specifically, we look at commercially available geological MoS_2 and molecular beam epitaxy-grown WSe_2 interfaced with an atomic layer deposited $Hf_xZr_{1-x}O_2$ ferroelectric. Our report will focus on the results of our investigations of this interface carried out using a combination of X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) techniques.

4:20pm **EM+PS+TF-MoA9 Electronic and Thermal Properties of 2D Materials**, ***Connor McClellan***, *E. Yalon, K. Smithe, C. English, S. Vaziri, C. Bailey, A. Sood, M. Chen, E. Pop,* Stanford University

This talk will present recent highlights from our research on two-dimensional (2D) materials and devices including graphene, and transition metal dichalcogenides (TMDs). The results span from fundamental measurements and simulations, to devices, to system-oriented applications which take advantage of unusual 2D material properties.

Using the low cross-plane thermal conductance, we found unexpected applications of graphene as an ultra-thin electrode to reduce power consumption in phase-change memory [1]. We have also demonstrated wafer-scale graphene systems for analog dot product computation [2]. We have grown monolayer 2D semiconductors by chemical vapor deposition over cm^2 scales on amorphous oxides, including MoS_2 with low device variability [3], WSe_2, and $MoSe_2$.

Using a self-aligned process, we demonstrated 10 nm gate-length monolayer MoS_2 transistors with excellent switching characteristics and approaching ballistic limits [4]. Using sub-stochiometric oxides, we achieved high electron doping to reduce electrical contact resistance down to 480 Ω·µm and increase on-current up to a record of 700 µA/µm in monolayer MoS_2 [5]. We also directly measured the saturation velocity in monolayer MoS_2, finding it is thermally-limited (i.e. by device self-heating and phonon scattering) to about one-third that of silicon and about one-tenth that of graphene [6]. Using Raman thermometry, we uncovered low thermal boundary conductance (~15 $MW/m^2/K$) between MoS_2 and SiO_2, which could limit heat dissipation in 2D electronics [7]. We are presently exploring unconventional applications including thermal transistors [8], which could enable nanoscale control of heat in “thermal circuits” analogous with electrical circuits. These studies reveal fundamental limits and new applications of 2D materials, taking advantage of their unique properties.

References: [1] A. Behnam et al., Appl. Phys. Letters. 107, 123508 (2015). [2] N. Wang et al., IEEE VLSI Tech. Symp., Jun 2016, Honolulu HI. [3] K. Smithe et al., ACS Nano 11, 8456 (2017). [4] C. English et al., IEEE Intl. Electron Devices Meeting (IEDM), Dec 2016. [5] C. J. McClellan et al., IEEE Device Research Conference (DRC), June 2017. [6] K. Smithe et al., Nano Lett. 18, 4516 (2018). [7] E. Yalon, E. Pop, et al., Nano Lett. 17, 3429 (2017). [8] A. Sood, E. Pop et al. Nature Comm. 9, 4510 (2018).

4:40pm **EM+PS+TF-MoA10 Electronics in Flatland**, ***Sanjay Banerjee***, University of Texas at Austin **INVITED**

2D materials such as graphene, transition metal dichalcogenides and topological insulators have opened up avenues in beyond-CMOS device concepts. We will discuss our work involving single or many-particle 2D-2D tunneling, leading to transistors with negative differential resistance. We also explore spintronics in these systems for novel logic and memory devices. We will also discuss the use of these materials in less esoteric, but more practical high frequency, mechanically flexible FETs for IoT applications.

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