Electronic Materials and Photonics Division
Room A214 - Session EM+AP+MS+NS+TF-ThM

Advanced Processes for Interconnects and Devices

Moderators: Andy Antonelli, Nanometrics, Bryan Wiggins, Intel Corporation

8:00am **EM+AP+MS+NS+TF-ThM1 High-density Plasma for Soft Etching of Noble Metals**, ***Gerhard Franz***, *V. Sushkov,* Munich University of Applied Sciences, Germany; *W. Oberhausen, R. Meyer,* Technische Universität München, Germany

During our research to define a contact which can be serve as thin hard mask in III/V semiconductor processing, we focused on the Bell contact which consists of Ti/Pt(Mo)/Au and chlorine-based plasmas generated by electron cyclotron resonance. For platinum, we identified PF_3 as main component which acts comparable to CO [1]. This fact triggered our search for suited etchants for gold and copper. For Au, the best ambient is a mixture of CH_4, Cl_2, and O_2 which is stabilized by Ar [2]. This mixture generates residual-free etching of metal films which are clearly free of "fencing" and "hear's ears."

The etching process has been established up to thicknesses of half a micron which is the typical thickness of metal films on the p-side of laser devices. With the aid of optical emission spectroscopy, the generation of CO could be proven [3]. This reagent seems to be the main component for real etching without residual fencing.

[1] G. Franz, R. Kachel, and St. Sotier, Mat. Sci. Semicond. Proc. **5**, 45 (2002)

[2] G. Franz, R. Meyer, and M.-C. Amann, Plasma Sci. Technol. **19**, 125503 (2017)

[3] G. Franz, W. Oberhausen, R. Meyer, and M.-C. Amann, AIP Advances **8**, 075026 (2018)

8:20am **EM+AP+MS+NS+TF-ThM2 Crystalline InP Growth and Device Fabrication Directly on Amorphous Dielectrics at Temperatures below 400°C for Future 3D Integrated Circuits**, ***Debarghya Sarkar***, *Y. Xu, S. Weng, R. Kapadia,* University of Southern California

A fundamental requirement to realize 3D integrated circuits is the ability to integrate single crystal semiconductor devices on the back-end of functional layers within a thermal budget of ~400 °C. Present state-of-the-art methods involve wafer bonding or epitaxial growth and transfer, since directly growing on amorphous materials by traditional epitaxial growth processes like MOCVD and MBE would give polycrystalline films with submicron-scale grains. To that end, a newly introduced and actively developing growth method called Templated Liquid Phase (TLP) has demonstrated the ability to achieve single crystal compound semiconductor mesas of areal dimension ~ 10um diameter on diverse amorphous substrates. While previous demonstrations of TLP growth were at temperatures around 500-600 °C, in this presentation we would discuss some of the recent material characteristics and device results achieved and insights obtained, for crystalline InP mesas grown on amorphous dielectrics at temperatures below 400 °C. InP nucleation and growth was obtained for temperatures 360 °C down to 200 °C. Morphological variations of the grown crystals observed under different growth conditions (temperature, pressure, precursor flux) and strategies to obtain compact macro-defect free crystal growth would be presented. Contrary to general expectation of poor optoelectronic quality at these lower temperatures, the room temperature steady-state photoluminescence shows peak position and full width at half maximum comparable to that of commercial InP wafer. External quantum efficiency is within an order of magnitude of single crystal commercial wafer at optimal growth conditions. Back-gated phototransistor was fabricated using low temperature InP grown directly on the amorphous gate oxide, and with all processing steps below the thermal budget of 400 °C. A typical device showed reasonable ON-OFF ratio of about 3 orders of magnitude, with peak responsivity of 20 A/W at V_{gs}=3.2V and V_{ds}=2.1V under an irradiance of 4 mW/cm^2 of broadband light. In summary, this technology could potentially open up a viable avenue to realize 3D integrated circuits by enabling integration of high performance electronic and optoelectronic devices on the back-end of functional layers within the acceptable thermal budget of 400°C.

8:40am **EM+AP+MS+NS+TF-ThM3 The Role and Requirements of Selective Deposition in Advanced Patterning**, ***Charles Wallace***, Intel Corporation **INVITED**

The edge placement error (EPE) margin on features patterned at tight pitches presents a difficult integrated challenge. Area selective deposition, chemically selective etches and the design of thin films for selectivity have risen to the top priorities in advanced patterning. The EPE control requirement creates a complex interaction between many integrated modules such as thin film deposition, etch (wet and dry), chemical-mechanical polish and lithography. The introduction of EUV lithography into the semiconductor patterning process has enabled some simplification of process architecture; however, has not decreased EPE margin enough to keep up with the pitch scaling requirements. Chemical selectivity is the most effective way to avoid EPE-caused failures on devices which lead to poor yield. Some of the limits to achieving selective growth solutions include development of self-assembled monolayers (SAMs), selective ALD/CVD growth and the metrology required to prove success. The development of manufacturable deposition chambers by the industry is a key requirement in order to adequately test the capability of these new process options.

9:20am **EM+AP+MS+NS+TF-ThM5 Graphene-Template Assisted Selective Epitaxy (G-TASE) of Group IV Semiconductors**, ***M. Arslan Shehzad***, *A. T. Mohabir, M.A. Filler,* Georgia Institute of Technology

As conventional 2-D transistor scaling approaches its limits, 3-D architectures promise to increase the number of devices and reduce interconnect congestion. A process able to monolithically integrate single-crystalline group IV materials into the back-end-of-line (BEOL) may enable such designs. Here, we demonstrate the graphene-template assisted selective epitaxy (G-TASE) of single-crystal Ge on amorphous substrates at temperatures as low as 250 °C. This work represents a significant step forward for TASE methods, which have been largely limited to III-V and II-VI materials, bulk crystal templates, as well as higher temperatures. We specifically grow Ge nanostructures on graphene-on-oxide at the bottom of nanometer-scale oxide trenches by leveraging differences in group IV atom sticking probability between graphene and oxide surfaces. Raman mapping confirms the single crystallinity of as-grown Ge crystals. Time-dependent studies show a linear increase in Ge crystal height even after emerging from the oxide trench, indicating Ge atoms preferentially adsorb to the top facet under our growth conditions. Our studies also reveal that G-TASE is sensitive to the plasma process used to expose graphene in the oxide trenches. This work extends TASE to a new, technologically-relevant materials system and provides fundamental insight into the underlying physicochemistry.

KEY WORDS: silicon, germanium, epitaxy, graphene, selective deposition

9:40am **EM+AP+MS+NS+TF-ThM6 Resistivity and Surface Scattering Specularity at (0001) Ru/dielectric Interfaces**, *S.S. Ezzat,* University of Central Florida; *P.D. Mani,* View Dynamic Glass, Inc.; *A. Khaniya, W.E. Kaden,* University of Central Florida; *D. Gall,* Rensselaer Polytechnic Institute; *K. Barmak,* Columbia University; ***Kevin Coffey***, University of Central Florida

In this work we report the variation of resistivity with film thickness and with changes in surface characteristics for ex-situ annealed single crystal (0001) Ru thin films grown on c-axis sapphire single crystal substrates. The room temperature deposition of SiO_2 on the Ru surface increased the resistivity of the annealed films and is interpreted as an increase in diffuse scattering of the upper surface from a primarily specular previous condition in the context of the Fuchs-Sondheimer model of surface scattering. The characterization of the films and upper Ru surface by low energy electron diffraction (prior to SiO_2 deposition), x-ray reflectivity, x-ray diffraction, and sheet resistance measurements is reported. The film resistivity and specularity of the Ru/SiO_2 interface is observed to reversibly transition between high resistivity (low specularity) and low resistivity (high specularity) states.

11:00am **EM+AP+MS+NS+TF-ThM10 Electrochemical Atomic Layer Deposition and Etching of Metals for Atomically-Precise Fabrication of Semiconductor Interconnects**, *Y. Gong, K. Venkatraman,* ***Rohan Akolkar***, Case Western Reserve University **INVITED**

Moore's law drives continued device miniaturization in nano-electronics circuits. As critical dimensions are approaching the single nanometer length scale, the semiconductor industry is seeking novel technologies for precisely tailoring materials and structures at the atomic scale. While vapor-phase, plasma-assisted techniques of atomic layer deposition (ALD)

and etching (ALE) are capable of providing nano-scale control over metal deposition and etching, these processes may not provide the requisite atomic-scale precision. Additionally, ALD precursors are unstable and often expensive. Thus, alternative solution-phase electrochemical processes are being developed in our laboratory. In our electrochemical ALD (e-ALD) approach, a sacrificial monolayer of zinc is first deposited on the noble substrate via underpotential deposition (UPD). The zinc adlayer then undergoes spontaneous surface-limited redox replacement (SLRR) by the desired metal such as Cu or Co. Sequential UPD and SLRR steps enable fabrication of multi-layered deposits in a layer-by-layer fashion. An analogous approach for electrochemical ALE (e-ALE) is also being developed. In electrochemical ALE of Cu, surface-limited sulfidization of Cu forms a cuprous sulfide (Cu_2S) monolayer. The sulfidized Cu monolayer is then selectively removed through spontaneous complexation of the Cu^{+1} in a chloride-containing etchant medium. The sequence can be repeated to etch bulk metal films one atomic layer at a time. This talk will highlight numerous advantages and fundamental characteristics of e-ALD and e-ALE processes and describe opportunities for integrating them in wafer-scale metallization applications.

12:00pm **EM+AP+MS+NS+TF-ThM13 Wafer-Scale Fabrication of Carbon-Based Electronic Devices***, **Zhigang Xiao**, J. Kimbrough, J. Cooper, K. Hartage, Q. Yuan,* Alabama A&M University

In this research, we report the wafer-scale fabrication of carbon nanotube or graphene-based electronic device such as field-effect transistors (FETs). Carbon nanotube-based devices were fabricated with the alternating electric field-directed dielectrophoresis (DEP) method, and the graphene-based devices were fabricated with the carbon films grown with plasma-enhanced atomic layer deposition (PEALD) or e-beam evaporation. Semiconducting carbon nanotubes were dispersed ultrasonically in solutions, and were deposited and aligned onto a pair of gold electrodes in the fabrication of carbon nanotube-based electronic devices using the dielectrophoresis method. The DEP-aligned tubes were further fabricated into carbon nanotube field-transistors (CNTFETs) and CNTFET-based electronic devices such as CNT-based inverters and ring oscillators using the microfabrication techniques. The fabricated devices were imaged using the scanning electron microscope (SEM) and high-resolution transmission electron microscope (HRTEM), and the electrical properties were measured from the fabricated devices using the semiconductor analyzer. The semiconducting CNTs achieved higher yield in the device fabrication, and the fabricated devices demonstrated excellent electrical properties.

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