Plasma Science and Technology Division
Room 104A - Session PS+EM-WeM

Advanced Patterning

Moderators: Jeffrey Shearer, IBM Research Division, Albany, NY, Yiting Zhang, KLA-Tencor

8:00am **PS+EM-WeM1 Study of High Selective Silicon Nitride Etching Mechanisms in Remote Plasmas: Impact of Wafer Temperature**, ***Emilie Prevost***, STMicroelectronics, France; *L. Vallier, G. Cunge,* LTM, Univ. Grenoble Alpes, CEA-LETI, France; *C. De Buttet,* CEA-LETI, France; *S. Lagrasta,* STMicroelectronics, France; *C. Petit-Etienne,* LTM, Univ. Grenoble Alpes, CEA-LETI, France

Nowadays in the Semiconductor industry, challenging applications often requires ultra-high selectivity etching processes. Wet processes are often used but have drawbacks and show limitations in high aspect ratio features. One alternative possibility is to use chemical downstream etching plasmas. In this work, NF_3/O_2 downstream plasmas are used to etch selectively Si_3N_4 towards SiO_2 in high aspect ratio patterns (over 100).

In NF_3/O_2 plasmas, we observe that the wafer temperature (T°) has a considerable (but non linear) impact on the etching selectivity. When T° is raised from 40°C to 100°C, the selectivity first drop and then increase again, with a marked minima at 70°C. Indeed, the etching rate of Si_3N_4 and SiO_2 have a different behavior with T°: while the SiO2 etch rate increase slowly and continuously with T°, the Si_3N_4 etch rate first drop between 40 and 70 °C and then increases again at higher T°. This effect is attributed to two mechanisms in competition, the etching led by atomic fluorine and surface passivation via oxidation. To better understand the nonlinear behavior of the Si_3N_4 etch rate, the etching mechanisms of Si_3N_4 as a function of T° was investigated by plasma (VUV absorption spectroscopy) and surface diagnostics (Ellipsometry,XPS and AFM).

Angular XPS analysis show that the Si_3N_4 surface oxidation is minimal at low T° (40°C). As the wafer T° is increased, the thickness of the oxidized layer also increases rapidly until it reaches its maximum (about 5 nm) at 70°C. This is attributed to an enhanced diffusion of the O atoms produce by the plasma in the Si_3N_4 material. At higher T° the thickness stays constant but the amount of O in the layer decreases. In the NF_3/O plasma, atomic fluorine are responsible for the etching of both Si3N4 and SiO2 but with a natural selectivity. Therefore, the surface oxidation of the Si_3N_4 surface during etching is going to slow down the nitride etch rate and the thicker this layer is the smaller the etch rate will be (F atoms must diffuse through this layer to reach Si_3N_4). Therefore, when the T° is increased the Si_3N_4 etch rate initially drops because the SiO_x layer at its surface becomes thicker. Above 70°C the layer thickness stays constant but its degree of oxidation is decreasing when T° is increased: this explain why the Si_3N_4 etch rate increases again above 70°C. Hence the nonlinear behavior of the selectivity is due to a competition between the etching (by atomic fluorine) and surface oxidation, which strongly depends on T°. We highlighted via our research an important change on the etching mechanism at 70 °C, explained by the rapid formation of a thick oxidized layer.

8:20am **PS+EM-WeM2 Mechanism of Highly Selective SiO_2 Etching over Si_3N_4 using a Cyclic Process with BCl_3 and Fluorocarbon Gas Chemistries**, ***Miyako Matsui***, Hitachi Ltd., Japan; *K. Kuwahara,* Hitachi High-Technologies Corp., Japan

Multiple patterning techniques require extremely high selectivity to various materials and controllability of cross-sectional pattern profiles with atomic scale precision. In these fine patterning techniques, SiO_2 etching over Si_3N_4 requires an advanced process to form a thinner protection layer on Si_3N_4. For example, SiO_2 atomic layer etching with the fluorocarbon (FC) passivation of C_4F_8 plasma followed by Ar^+ bombardment has been investigated [1]. To achieve a high selectivity to Si_3N_4 using conventional FC plasma, the thickness and composition of the FC film should be controlled to protect only the Si_3N_4 surface from reaction with the FC film [2]. In our previous study, we proposed a cyclic SiO_2 etching process over Si_3N_4 by using BCl_3 and FC gas chemistries [3]. BCl_3 plasma was applied because it was expected to form a thin protection layer, which was suitable for selective etching at fine patterns when a low wafer bias was used. The thin protection layer formed by BCl_3 plasma was also expected to inhibit the spontaneous etching of Si_3N_4 by F radicals.

In this study, we investigated a cyclic process using BCl_3 and fluorocarbon gas chemistries for a fine pattern structure with a space width of 20 nm. The relationships between etching parameters and cross-sectional pattern profiles were also analyzed to control the pattern profiles. This process alternately performs two steps: an adsorption step using BCl_3 mixed-gas plasma and an etching step using BCl_3/CF_4/Ar plasma with applying a wafer bias. The mechanism of the cyclic process was investigated by analyzing the surface chemistry at each step. At the adsorption step, a thicker BCl_x layer was formed on the Si_3N_4 surface than on the SiO_2 surface. Then, CCl_x films were formed on both surfaces at the etching step. We found that the thicker BCl_x layer formed on Si_3N_4 at the adsorption step protected Si_3N_4 from etching by reaction of BCl_x with CF_x and F radicals at the etching step. The B atoms in the BCl_x layers desorbed from the surfaces by forming BF_x, BCl_xF, and CCl_x. In contrast, the BCl_x layer became thinner on SiO_2 than that on Si_3N_4 to promote ion-assisted etching of SiO_2. This is because the BCl_x component has high reactivity with SiO_2, and the CF_x component was also consumed by the etching reaction with SiO_2. We also found that ion-flux should be controlled to etch without shoulder-loss, and ion-energy should be controlled to etch without footing shape at the bottoms of the pattern.

[1] D. Metzler et al., J. Vac. Sci. Technol. A **32**, 020603 (2014).

[2] M. Matsui et al., J. Vac. Sci. Technol. A **19**, 2089 (2001).

[3] M. Matsui et al., Jpn. J. Appl. Phys. **57**,(2018) to be published.

8:40am **PS+EM-WeM3 DSA Patterning for and Beyond CMOS**, ***Patricia Pimenta Barros***, CEA-LETI, France; *N. Posseme,* CEA, LETI, France; *S. Barnola,* CEA-LETI, France; *R. Tiron,* CEA-LETI, MINATEC, France; *A. Gharbi, MA. Argoud, Z. Chalupa, M.-G. Gusmao-Cacho,* CEA-LETI, France; *A. Paquet,* Arkema, France; *F. Delachat,* CEA-LETI, France; *C. Nicolet, C. Navarro,* Arkema, France **INVITED**

The continuous increase of CMOS device density has led to new 3D architectures. For the sub-7nm nodes, Leti investigates the interest of Tri-gate, Ω-gate and stacked nanowires architectures for better electrostatic control at aggressive dimensions [1, 2]. These new architectures bring a set of etching challenges at the integration level (from active, spacer, Si/SiGe removal) and require innovative etching solutions, such as gas or bias pulsing and atomic layer etching (ALE). In this paper, an overview of the main challenges and solutions for Si/SiGe stacked NW patterning will be exposed.

The active patterning of dense stacked nanowires have been already demonstrated by Leti using the Sidewall Image Transfer (SIT) technique [3]. In this paper, we will focus on the Directed Self Assembly (DSA) of block-copolymers (BCPs) that is considered as a cost-effective and complementary solution to conventional or EUV lithography [4, 5]. Herein, stacked Si nanowires are patterned using a DSA UV-assisted graphoepitaxy approach. Chemoepitaxy and graphoepitaxy approaches, which are the two ways to perform DSA, will be benchmarked. The transfer of ultra-small patterns using high-chi BCPs materials (pitch <20nm) will be also reported.

Based on LETI's FDSOI background, we are investigating new architectures such as steep slope devices, mechanical switches or single electron devices in a CMOS compatible flow. They are all studied in a CMOS co-integration perspective to enable the hybrid logic field [6]. In this paper, we will show that DSA patterning could be a good candidate for some applications beyond CMOS such as Single Electron Transistor devices or nano-membranes manufacturing.

[1] Coquand, R., et al., Symposium on VLSI Technology, pp. T226-T227 (2013)

[2] Barraud, S., et al., Symposium on VLSI Technology, Kyoto, pp. T230-T231 (2013)

[3] Gaben, L., et al., International Conference on Solid State Devices and Materials, 1108 - N-2-2, pp1108-1109 (2015)

[4] Jeong, S-J., et al., Materials today 16 (12), 468-476 (2013).

[5] Guerrero, D. J., Solid State technology (2017)

[6] Barnola, S, et al., Proc. SPIE 9054 (2014)

9:20am **PS+EM-WeM5 Composition Modulation of SiGe for Si/SiGe Dual Channel Fin Application**, ***Yohei Ishii***, Hitachi High Technologies America Inc.; *Y.-J. Lee,* National Nano Divice Laboratories; *W.-F. Wu,* National Nano Device Laboratories; *K. Maeda,* Hitachi High Technologies America Inc.; *H. Ishimura,* Hitachi High-Technologies Taiwan Corp.; *M. Muira,* Hitachi High-Technologies Corp.

As a consequence of downscaling to follow Moore's law, device structure was changed from conventional planar structure to Fin-type Field Effect Transistors (FinFETs) to achieve higher drive current and lower leakage current. In sub-10nm processes, it is necessary to further improve FinFETs electrical performance. A promising approach is to replace silicon fins with

a new material, such as silicon germanium, which enhances carrier mobility [1]. In Si/SiGe dual channel FinFETs, Si is used in n-FETs, while SiGe is used in p-FETs. Therefore, it is necessary to understand the difference in etching characteristics between Si and SiGe. Recently, we have developed an etching process to selectively etch Si over SiGe, and proposed the etching mechanism [2]. This etching technique proved to adjust not only the Si and SiGe pattern CDs (Si CD> SiGe CD and vice versa), but also Si and SiGe etched depth (Si etched depth < SiGe etched depth and vice versa), using Si/SiGe dual channel fin pattern samples.

As for the electrical performance of SiGe, it is important to form Si-rich SiGe surface at the SiO2/SiGe interface, because interface states play important role on sub-threshold characteristics [3]. There are several methods to form Si rich surface, such as thin Si cap epitaxial growth over SiGe fin [4] or H2 anneal-induced Si segregation [5]. However, it remains difficult to achieve the surface without the formation of a thick Si layer, which acts as a parasitic channel. In addition to that, avoiding Ge diffusion into Si cap layer is also an issue.

In this presentation, we propose a low-temperature process for achieving atomically controlled Si rich surface by utilizing plasma treatment to induce SiGe composition modulation at SiGe surface. We will also present a method to flexibly control the composition of SiGe surface (from Ge-rich surface to Si-rich surface) by utilizing plasma treatments. Details of the study will be discussed in this presentation.

[1] D. Guo, et. al., VLSI Tech. Dig., p.14, 2016

[2]. Y. Ishii et. al., Jpn. J. Appl. Phys. (Accepted)

[3]. C. H. Lee et. al., IEDM Tech. Dig., p.31.1.1., 2016

[4]. H. Mertens, et al., VLSI Tech. Dig., p.58, 2014

[5] L. Rudkevich, et. al., Phys. Rev. Lett. Vol.81 p. 3467 (1998)

9:40am **PS+EM-WeM6 Etching Mechanisms of Si Containing Materials in Remote Plasma Source using NF3 based Gas Mixture***, **Erwine Pargon**, V. Renaud, C. Petit-Etienne, L. Vallier, G. Tomachot, G. Cunge, O. Joubert,* Univ. Grenoble Alpes, CNRS, LTM, Grenoble, France*; J.-P. Barnes, N. Rochat,* Univ. Grenoble Alpes, CEA, LETI, Grenoble , France

The introduction of new 3D designs (fin FETs, nanowire..) for sub-10 technological nodes bring new challenges for etch applications. Contrary to planar devices, 3D devices require more isotropic etch capabilities with high selectivity between different materials . Remote plasma source (RPS) which is based only on chemical mechanisms offers great capability for etch applications requiring high etch selectivity such as removal of SiN spacer in 3D device or fabrication of Si or SiGe horizontal nanowire for gate all around device. NF3 based gas mixtures are frequently used to etch Si containing materials in a RPS process. In this paper, we propose to investigate the etching and selectivity mechanisms of Si containing materials (SiN, SiO_2, SiGe and Si) in RPS process using NF3/NH3 or NF3/H2 gas mixture. In this study, the hydrogen content of SiN and SiO_2 materials is modulated by using different deposition techniques (LPCVD, PECVD..). The etching experiments are performed in an industrial RPS reactor. The substrate temperature can be varied between 40 and 200°C. The etching kinetics are in real time thanks to in situ kinetic ellipsometry. The results show that the etching of both SiN and SiO_2 materials in NH_3/NF_3 remote plasma proceeds through the formation of $(NH_4)_2SiF_6$ salts on the material surface that consume the pristine material. Similarly to oxidation processes, the consumed thickness of material is proportional to the thickness of the salt layer. The real time monitoring of the SiN and SiO_2 etching reveals that the etching proceeds in three phases. First, the reactive species absorb on the material surface but without consuming it. The delay before the materials starts to be etched increases with substrate temperature and decreases if the surface is rich in O and/or H, conveying that these elements act as a catalysis of the salt formation. During the second phase, the material is etched rapidly through the salt layer. During this phase, the material consumption depends on the substrate temperature and nature, as well as the plasma conditions. Finally during the third phase, the materials are consumed less rapidly because the reactive species have to go through the salt layer before reaching the salt/material interface. The etching kinetics in the third phase are almost independent on the substrate temperature, material, and plasma conditions. The key to get infinite etch selectivity of SiN over SiO_2 and SiO_2 over SiN is to tailor the substrate temperature and the surface functionalization. High etch selectivity of SiGe over Si can be easily achieved in NH3/NF3 remote plasma. Adding H2 in the mixture allows to reverse the trend.

11:00am **PS+EM-WeM10 Precise Control of Silicon Nitride Spacer Etching Selectively to Silicon for 3D CMOS Device***, V. Ah-Leung, N. Possémé, **Olivier Pollet**, S. Barnola,* CEA-LETI, France

With transistors size scaling down, device processing requirements become more and more stringent. For technology node beyond 14 nm, one of the most critical step is the spacer etching. It requires a perfect anisotropy (no CD loss) without damaging [1] nor consumption of the exposed material like silicon, silicon germanium and oxide [2,3]. In planar transistor, the silicon or silicon germanium consumption is limited by the short over-etch process (30-50%). However for vertically stacked wires3D devices, the silicon fin is directly exposed during the removal of the silicon nitride on the active area sidewalls. This is the major issue since in this case, important over etch is required (>200%) to fully remove the residues at the bottom of the fin. Therefore, the spacer etch is considered today as one of the most challenging etch process for 2D but more especially 3D devices.

Today, current fluorocarbon etch chemistry (like CH3F/CH4/O2) are no longer suitable for 3D CMOS integration where long overetch is necessary.

In this context, we propose to introduce a new cyclic etch process of silicon nitride selectively to silicon to fulfill the stringent etch requirements described above [4].

This cyclic process is composed of two steps. A first step consists in silicon nitride etching till to top of the silicon fin. XPS analyses performed on blanket films (Silicon nitride and Si) reveal that a thin reactive layer is formed at the SiN surface, while an important deposition is observed at Si surface. This deposition at the Si surface is dependent of the process time. A second step (CHF3 based chemistry) allows partially removing the deposition on top of Si while etching the silicon nitride. Thanks to this new approach silicon nitride is linearly etched as a function of the number of cycles while the silicon film consumption is below 1.5nm. The selectivity reached by this new process is >100.

The impact of the different process step times and number of cycles on SiN and Si surface composition has been analyzed by XPS and will be presented. A proof of concept on vertically stacked wires patterned wafer will show that the silicon nitride spacer can be fully removed on the sidewall of the fin with limited impact on the silicon consumption/damage.

[1] N. Kuboi, T. Tatsumi, T. Kinoshita, T. Shigetoshi, M. Fukasawa, J. Komachi, and H. Ansai, J. Vac. Sci. Technol. A **33** (6), 061308 (2015).

[2] B. E. E. Kastenmeier, P. J. Matsuo, and G. S. Oehrlein, J. Vac. Sci. Technol. A **17** (6), 3179 (1999).

[3] K. Eriguchi, Y. Nakakubo, A. Matsuda, Y. Katao, K. Ono, IEEE Electr. Device L. **30** (7), 712 (2009).

[4] N.Posseme, S.Barnola, patent pending

11:20am **PS+EM-WeM11 A Study on the Distortion of Poly Si Nano Hole Profile with High Aspect Ratio in sub X nm***, **Jin Won Lee**, J.Y. Lee, K.J. Seong, T.S. Kwon, H.H. Jeong, S.S. Hong, D.W. Han, B.R. Lim, A.R. Ji, Y.M. Oh, J.C. Park,* Samsung Electronics, Republic of Korea

As the Critical Dimension (CD) of Semiconductor becomes smaller, process using new materials is being developed and multi-patterning processes are required to overcome the limitations of lithography. However, only a few of them have been adapted to mass-production of the semiconductor because they costs highly and are complex. As a result, Researches on Si materials (SiN, SiO_2, Poly-Si) widely used in semiconductors have been actively conducted.

In this study, we will describe the etch process with excellent LER (~ 1) by removing the distortion which causes various problems and securing the vertical profile in the Poly-Si nano hole with the high aspect ratio (1:50) in sub X nm. HBr based Etch is favorable for Poly Si Etch because it has a high selectivity between Poly-Si and SiO_2. However it has tendency to cause clogging $Si_xBr_yO_z$ byproducts which aggravate the open margin and profile control. By the way, the etch profile is also deteriorated due to irregularly crystallized grains, which is a character of Poly-Si and they might induce etch stop it is severe. Unlike HBr based etch, Cl2 based etch tends to be less polymerizing and less reactive thus it causes less clogging which is less effective by the poly grain and is effective to improve the profile. We adopted Cl2 based multi cycle etch over HBr based etch to secure the characteristics of the vertical profile with etch stop free.

Distortion must be solved in order to improve the LER, which is an important factor that affects not only the vertical profile but also the electrical characteristics of semiconductor of device. In general, the etch rates increases with increased process temperature and the distortion tends to be improved. However, in our study, the hole distortion is

improved and more vertical profile is led at low temperature. This can be explained by the difference in the re-deposition tendency of byproduct. When the temperature is high, a large amount of byproduct, that occurs after etch, is more re-deposited on the upper part than the lower part because the convective phenomenon becomes more active and the sticking coefficient of the hole side wall decreases. As a result, the clogging becomes worse, and the hole side wall cannot be re-deposited uniformly. CD tends to be smaller. Profile tends to be positive and LER tend to be worse. On the contrary, if the process temperature is low, the sticking coefficient of the hole side wall increases, and the re-deposition is performed well. Since it is totally re-deposited in the hole side wall, it is confirmed the CD is increased and a vertical profile is foamed and the LER is improved.

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11:40am **PS+EM-WeM12 Etching Recipe Optimization Using Machine Learning**, ***Takeshi Ohmori***, *H. Nakada, M. Ishikawa, N. Kofuji, T. Usui, M. Kurihara,* Hitachi, Ltd., Japan **INVITED**

The development of semiconductor fabrication processes has been prolonged due to constantly evolving nano-scale 3D devices. This lengthy development period has driven up the cost of semiconductor devices, and the process development needs to be sped up in order to reduce the cost.

Along with time modulation of plasma generation and bias power and an increase in the number of gas species, continuous improvement of the control functions of a plasma etcher has been made to provide accurate nano-scale etching. A set of parameters for the control functions is called a recipe, which is used as input data for the etcher. Etching accuracy can be improved by increasing the number of parameters in the recipe. However, it is difficult to optimize the recipe for obtaining a target etch profile when there are many parameters.

In this work, we present two types of exploration method for recipe optimization using machine learning: one using etching profile data [1] and the other using feature data related to the etching profile [2]. These were developed to assist the development of the etching process and to reduce the time period of the development, respectively.

In the method using the profile data, a recipe is optimized through the repetition of an optimization cycle that consists of learning the relationship between the profiles and the recipes, predicting the recipes to obtain a target profile, performing etching experiments with the predicted recipes, and adding the experimental results to the learning data. In this cycle, kernel ridge regression is used as the learning engine and a Si trench pattern is used to examine the exploration method. By using the predicted recipe, a vertical trench profile was successfully etched, and the profile was further improved by increasing the number of cycles from one to seven.

Next, we developed the recipe exploration method based on machine learning of feature data related to the etching profile in order to accelerate the optimization. A micro/macro cavity method is used to extract the feature data. An approximate region to obtain the vertical profile can be determined in the feature data space because the feature data show the characteristics of ion assist etching and radical etching. The relationship between the feature data and the recipes was learned, and feature data were then explored to obtain the vertical profiles. After the iteration of the exploration, it enabled us to determine the optimum recipes for the vertical profile in just seven times of Si trench etching.

[1] T. Ohmori et al., Proc. of Int. Symp. Dry Process, Tokyo, pp. 9–10 (2017).

[2] H. Nakada et al., Proc. Gaseous Electronics Conf., Pittsburgh (2017).

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