Wednesday Afternoon, October 24, 2018

Plasma Science and Technology Division
Room 104C - Session PS+EM-WeA

Advanced BEOL/Interconnect Etching

Moderators: Michael Morris, Trinity College Dublin, Tetsuya Tatsumi, Sony Semiconductor Solutions Corporation

2:20pm **PS+EM-WeA1 Etch Strategies for Reducing Defects and Pattern Roughness in BEOL EUV Patterning***, **Jeffrey Shearer**,* IBM Research Division, Albany, NY*; A. Raley, Q. Lou, J. Kaminsky,* TEL Technology Center, America, LLC*; L. Meli,* IBM Research Division, Albany, NY

As EUV lithography takes center stage in next-node semiconductor logic manufacturing, many challenges still need to be overcome. Of those, resist scumming, resist line breaks, and pattern roughness stand out as three of the top issues to address, especially when direct printing single levels below 36nm pitch. Previously, we have reported several methods of addressing these concerns in BEOL patterning, including introducing new material stacks and implementing new etch techniques such as resist reinforcement and quasi-atomic layer etching (QALE). This presentation will expand upon those ideas as well as introduce new etch methods that help enable direct EUV printing of single levels. Resist scumming will be addressed by exploring different types of descum etch chemistry. Data will show that line breaks can be reduced by resist reinforcement methods using pre-etch in situ deposition, increasing etch selectivity using QALE, and implementing direct current superposition (DCS). Additionally, we will show how line end pullback can be modulated with these different techniques and data will be presented that show resist reinforcement methods can recover more than 50% of line end pullback caused by more selective etch chemistries. The aspect ratio dependence of resist reinforcement and QALE will be discussed along with how aspect ratio impacts pattern roughness. The effectiveness of all of these etch strategies will be evaluated with defect characterization (bridge patterns and line breaks) and electrical testing (shorts and opens yield). Finally, we will discuss the impact of chamber configuration on EUV lithography pattern transfer. Data will be shown from chambers with the radio frequency (RF) split between top and bottom electrodes, dual RF on the bottom electrode only, and RF split between top and bottom electrodes with the addition of DCS. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

2:40pm **PS+EM-WeA2 Influence of Topological Constraints on the Ion Damage Resistance of Low-*k* Dielectrics***, **Qing Su**,* University of Nebraska-Lincoln*; T. Wang, J. Gigax, L. Shao,* Texas A&M University*; W. Lanford,* University at Albany*; M. Nastasi,* University of Nebraska-Lincoln*; L. Li,* Intel Corporation*; G. Bhattarai, M.M. Paquette,* University of Missouri-Kansas City*; S.W. King,* Intel Corporation

Low-*k* dielectric materials are well known to be sensitive to process induced damage during back-end-of-line (BEOL) patterning and metallization. This sensitivity has been largely attributed to the incorporation of terminal organic groups into the structure of low-*k* dielectric materials to lower dielectric permitivity and the subsequent loss of the terminal organic groups during BEOL processing. However, the correlations between the actual atomic structure of low-*k* dielectrics and their susceptibility to BEOL damage have been largely qualitative. A more quantitative metric for relating both the atomic structure and network topology of low-*k* dielectrics to downstream processing would allow for more efficient design and selection of materials for BEOL as well as pitch division multi-pattern applications.

Toward this end, we have investigated the ion radiation damage resistance for a series of low-*k* and high-*k* dielectric amorphous hydrogenated silicon carbide (a-SiC:H) thin films, wherein atomic structure and topological constraints have been previously shown to play a remarkably fundamental role in determining the full spectrum of electrical, optical, thermal, and mechanical properties. We specifically show the response of a-SiC:H films with > 37% hydrogen content and mean atomic coordination ($\langle r \rangle$) ≤ 2.7 subjected to 120 keV He^+ irradiation with damage level to 1 displacment per atom (dpa). Significant hydrogen loss, bond rearrangement, and mechanical stiffening were induced in these films. In contrast, comparatively minor changes were observed for a-SiCH films with <35% hydrogen content and $\langle r \rangle$ > 2.7 also exposed to the same He^+ irradiation. The observed radiation hardness threshold at $\langle r \rangle_{rad}$ > 2.7 is above the theoretically predicted rigidity percolation threshold of $\langle r \rangle_c$ = 2.4. As we will show, the higher observed radiation hardness threshold can be interpreted as evidence that terminal hydrogen bonds and bond bending forces associated with two-fold coordinated motifs are too weak to function as constraints in collisions with high energy ions. Eliminating these constraints from consideration would increase $\langle r \rangle_c$ to > 2.7 in agreement with the observed $\langle r \rangle_{rad}$ = 2.7. These results demonstrate the key role of network coordination and topological constraints in ion damage resistance and perhaps provides new criteria for the design of new ion damage resistant / tolerant materials.

3:00pm **PS+EM-WeA3 BEOL Patterning Challenges for 14nm and Beyond High Volume Manufacturing***, **Xiang Hu**,* GLOBALFOUNDRIES*; Y. Ren,* GLOBALFOUDRIES*; D. Medeiros, P. Lee,* GLOBALFOUNDRIES **INVITED**

As the semiconductor features progressively shrink to sub 20 nm dimensions, patterning technology becomes significantly more critical. Pattern fidelity, yield, quality and cost now all incrementally become competing factors to the successful production of advanced technology nodes in high volume manufacturing. In this paper we will provide an overview on the challenges of patterning technology for single patterning, double patterning (DP), triple patterning (TP), self-aligned double patterning and EUV patterning, based on the learning of BEOL (Back End of Line) patterning technology development. We will focus on BEOL patterning technology challenges for 14nm high volume manufacturing, and demonstrate the patterning solutions for DP and TP 1D and 2D structure optimization. We will elaborate on process enhancements and controls such as CD, tip-to-tip and iso-dense loading optimization, the integrated patterning solution for open and short yield improvement and via-to-metal reliability improvement, the multi-variant APC control for process stability improvement by APC thread reduction and thread sharing among a variety of products. The success of BEOL patterning technology is dependent on patterning capability, process robustness and cost of patterning solutions.

4:20pm **PS+EM-WeA7 Innovative Approaches for Future Challenges in MOL/BEOL Etch***, **Ryukichi Shimizu**,* Tokyo Electron Miyagi Limited, Japan **INVITED**

Critical dimensions (CD) continue to shrink driven by the quest for cheaper, faster and less power-consuming devices. If simple shrink was not enough, all of the back end, middle and front end of line (BEOL, MOL and MOL) also have introduced structural complexity and stringent topographic dimension, material property integrity and fundamental integration yield requirements. Self-aligned contact (SAC), high aspect ratio contact (HARC) and damascene structures in the MOL and BEOL typify challenging integrations. SAC structures are formed by oxide being etched from a nitride encasement. The oxide must be etched both beside and over thin (few nm) nitride films with near infinite selectivity as horizontal nitride layers can be exposed far before the deepest oxide in contact vias are removed. These structures are subject to “plugging” if the films get to thick, loss of nitride if the films get too thin, and etch rate or profile integrity loss elsewhere due to imbalances in ion energy flux or radical loss due to shadowing in a deep via. Obtaining the perfect balance of radical flux, ion flux and ion energy for these structures over a single die, let alone an entire wafer full of dies, is nearly impossible. Put in more general terms, fabrication challenges for plasma etch related to controlling local CD Uniformity (LCDU) and mitigating depth loading and CD loading are ever present due to difference in aspect ratio dependence (ARD) of transport of radicals and ions (and their energy) in features.

Atomic layer etching (ALE) has gained favor as an approach to extract more control over the fabrication of small CD complex topographic structures. The idea is that alternating steps of self-limiting processes (e.g., passivation layer formation) and desorption (e.g., the removal of a passivation layer) mitigate aspect ratio dependence effects that lead to the aforementioned problems. The problem is that not all passivation processes are self-limiting. Fluorocarbon based processes are not self-limiting rendering them quasi-atomic layer etch. Without special consideration, quasi-ALE has the same problems that continuous processes possess.

We have demonstrated the use of a new method of rapid advanced cyclic etch (RACE) comprising an isotropic CD trim step, mixed mode CVD, ALD and anisotropic bombardment to perform aspect ratio independent deposition and thereby eliminate CD bias effects. We show that X-Y CD control by ALD, CVD and trim can also be influenced by line-of-sight re-deposition from feature bottom. The ability to manage CD will be discussed as a means of enabling advanced patterning processes for both logic, interconnect and memory at advanced technology node.

5:00pm **PS+EM-WeA9 Gas-phase Pore Stuffing for Low-damage Patterning of Organo-silicate Glass Dielectric Materials***, **Jean-Francois de Marneffe**,* IMEC, Belgium*; M. Fujikama, T. Yamaguchi, S. Nozawa, R. Niino, N. Sato,* Tokyo Electron Technology Solutions Limited*; R. Chanson, K. Babaei Gavan,* IMEC, Belgium*; A. Rezvanov,* IMEC, Belgium/Moscow Institute of Physics and Technology*; F. Lazzarino, Z. Tokei,* IMEC, Belgium

Capacitance gain remains of high value for lowering the interconnect RC delay in CMOS transistors, especially in the current design-technology co-optimization (DTCO) era where circuit density is maximized. In view of their superior mechanical properties, intermediate low-k dielectrics (sub-nanometer pore diameter, open porosity < 20%, k-value > 2.5) do attract nowadays most interest. CVD porous organo-silicate glasses are the most industry-relevant materials. They do suffer from processing damage, due to their porous and bi-component nature. As a consequence, some tailored protection strategies need to be developed. The gas-phase pore stuffing (GPPS) is a CVD method using two organic reactive precursors. Vaporized monomers (Gases A and B) are injected into the reactive chamber, supplied to the substrates and polymerized. Polymers are formed in the pores, deep in the bulk dielectrics, and can be removed by thermal annealing in controlled atmosphere. The GPPS technique is demonstrated on multiple OSG materials (various porosity), then applied to an OSG dielectric with nominal k-value 2.55, porosity ~ 16% and pore diameter ~ 0.8nm, which is embedded into a M1/V0 45nm ½ pitch vehicle. The target patterning sequence aims at creating a dual damascene structure by the fully self-aligned via approach (FSAV). The benefits of the GPPS is studied on the various plasma steps used in the FSAV patterning, allowing to reduce plasma damage up to 50% for the most damaging part of the FSAV patterning sequence (CO_2 ash, used for post-via strip, GPPS recess and GPPS unstuffing). The ability of the GPPS to form a protective plug is demonstrated, by excess polymerization in the pre-patterned via. By taking advantage of the specific properties of the GPPS approach, modifications of the FSAV patterning sequence are proposed, leading to potentially large capacitance gain. Various unsealing, unplugging and unstuffing options will be described, aiming at preparing the low-k surface for GPPS stuffing, and/or restoring the original porosity without residues, at the end of the patterning sequence. The gain in low-k dielectric properties, using the GPPS technique, is studied by k-value extraction on the various used vehicles.

Dr R. Chanson has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 708106.

5:20pm **PS+EM-WeA10 ALD-Sequential Etch to Address Advanced BEOL Etch/Integration Challenges***, **Xinghua Sun**, Y.-T. Lu, K. Lutker-Lee, A. Raley,* TEL Technology Center, America, LLC*; D. O'Meara,* Tokyo Electctron, America, Inc.*; T. Yamamura,* Tokyo Electron Miyagi Limited*; Y. Kikuchi,* TEL Technology Center, America, LLC

As semiconductor nodes continue to scale past 7nm and beyond, control of critical dimension (CD), reactive ion etch (RIE) lag, low-k damage, material selectivity and chamfer profile becomes increasingly challenging for patterning of low-k materials in back end of line (BEOL) dual damascene processes. While modulation of plasma processing can address some of these challenges, process knobs that benefit one parameter can come into conflict with another, thereby leading to a necessity to compromise between them.

Recently, the introduction of anisotropic sequential etch, in which cyclical alternation of separated deposition and activation (etching) steps are used to decouple and control plasma chemistry, has revealed additional flexibility in profile control. However, anisotropic sequential etch tends to benefit processes that require significant boosts in etch selectivity and a controlled directional etch rate, while showing little improvement for processes where material damage is also a major concern, as in the case of low-k. As such, alternative methods to protect the low-k sidewall/corner during dual damascene processing are necessary. Introduction of a conformal, sacrificial side wall/corner protective layer through atomic layer deposition (ALD) can potentially fill this gap. Addition of an ALD-sequential etch process allows for a wide range of deposition choices, in contrast to the limited options generated through the gas chemistries typical for plasma etch. In this talk, we show how an ALD-sequential etchcan address dielectric etch challenges.

5:40pm **PS+EM-WeA11 The Underlying Role of Mechanical Rigidity and Topological Constraints in Reactive Ion Etching of Amorphous Materials***, **Gyanendra Bhattarai**, S. Dhungana, B.J. Nordell, A.N. Caruso, M.M. Paquette,* University of Missouri-Kansas City*; W. Lanford,* University at Albany*; S.W. King,* Intel Corporation

In order for self-aligned multi-pattern techniques to be extended deep into the single digit nanometer range, new fab friendly material combinations with near perfect etch selectivity will need to be identified. This in turn requires a greater understanding of the interplay between plasma etching processes and the properties of the material being etched. While some qualitative correlations between dry etch rates and material properties such as composition, porosity, and density have been reported, more quantitative relationships have been generally lacking. In this regard, we demonstrate that analytical expressions derived to describe the material dependence of the yield for ion-induced sputter processes can be extended to reactive ion etch processes. Specifically, we first demonstrate a direct relationship between the atomic surface binding energy (U_{sb},), bulk modulus, and ion sputter yield for the elements, and then subsequently prove our hypothesis for amorphous multi-element compounds by demonstrating that the same relationships exist between the reactive ion etch (RIE) rate and nanoindentation Young's modulus for a series of a-SiN_x:H and a-SiO_xC_y:H thin films. The impact of a materials network topology is further revealed via application of the Phillips–Thorpe theory of topological constraints, which directly relates Young's modulus to the mean atomic coordination ($<r>$) for an amorphous solid. The combined analysis allows the observed trends and plateaus in the RIE rate versus modulus to be ultimately reinterpreted in terms of the atomic structure of the target material through consideration of $<r>$. These findings establish the important underlying role of mechanical rigidity and network topology in ion–solid interactions and provide a new consideration for the design and optimization materials for self-aligned pitch division / multi-pattern technologies.

6:00pm **PS+EM-WeA12 Plasma Processing of Phase Change Materials for PCRAM***, N.D. Altieri, **Ernest Chen**, J.P. Chang,* University of California, Los Angeles*; S.W. Fong, C.M. Neumann, H.-S. Wong,* Stanford University*; M. Shen, T.B. Lill,* Lam Research Corporation

The manipulation of the amorphous to crystalline phase transition observed in chalcogenide glasses for non-volatile memory applications has been studied for many years since its initial conception. However, only recently has innovation in both materials development and memory device architecture enabled phase change random access memory (PCRAM) to become a promising candidate for applications such as neuromorphic computing.

Understanding the effects of plasma processing as well as post-processing damage of the phase change material (PCM) utilized in PCRAM is crucial to ensuring proper device performance. The studies presented herein focus on the behavior of $Ge_2Sb_2Te_5$ (GST-225) in conjunction with H_2 and CH_4 discharges as well as the roles of O_2 and N_2 through the use of a custom-built integrated ion beam chamber, inductively coupled plasma reactor, and *in-situ* x-ray photoelectron and quadrupole mass spectrometers.

Etch and gas phase reaction byproducts for single element Ge, Sb, and Te as well as GST-225 in hydrogen and methane have been identified through the use of quadrupole mass spectrometry and optical emission spectroscopy. X-ray photoelectron spectroscopy has been used to characterize surface bonding states and film composition across a wide parameter space, including low and high pressures as well as varying feed gas compositions.

Methane and hydrogen-based discharges were identified as capable GST etchant chemistries, resulting in rates up to 80 nm/min; however, the post-processing film composition was found to be strongly dependent on the chosen etch chemistry. Hydrogen radicals were identified as the dominant etchant species and resulted in the preferential removal of Sb and Te at low (15 mTorr) and high (75 mTorr) pressure conditions through the formation of volatile hydride products. Post-processing surface analysis indicated a substantial decrease in Sb and Te concentration from their initial 22 and 55 atomic percent to 3 and 4 atomic percent as well as an accumulation of Ge on the post-etch surface. Tuning of the etch chemistry was further explored through the use of auxiliary N_2 in order to modify the etch rate and preserve the starting 2:2:5 stoichiometry crucial to proper PCRAM device performance.

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