## Thin Films Division
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## Thin Films for Microelectronics
**Moderators:** Erwin Kessels, Eindhoven University of Technology, The Netherlands, Adrie Mackus, Eindhoven University of Technology, The Netherlands

8:00am **TF+EM+MI-WeM1 Electrode Modulated Electric Field Capacitance Nonlinearity in ALD $Al_2O_3$ and $HfO_2$ Metal-Insulator-Metal Capacitors**, *D.Z. Austin, K. Holden,* ***John Conley, Jr.***, Oregon State University

Back-end-of-line metal-insulator-metal capacitors (MIMCAPs) require increasing capacitance density ($C_{ox}$) while maintaining low leakage current density ($J_{leak}$). In addition, analog and mixed signal (AMS) applications are particularly sensitive to nonlinearity of capacitance-voltage (CV), empirically characterized by the quadratic voltage coefficient of capacitance, $\alpha_{VCC}$. Scaling of MIMCAPs for AMS applications is increasingly challenging as $C_{ox}$, $J_{leak}$, and $\alpha_{VCC}$ are all inversely proportional to dielectric thickness ($d_{ox}$). Despite its technological importance, the fundamental mechanisms responsible for $\alpha_{VCC}$ are not fully understood. It is well established that the "bulk" dielectric material has a dominant effect, where $\alpha_{VCC}$ increases with increasing dielectric constant and roughly as $1/d_{ox}^2$. However, the influence of the electrode interfaces is not currently understood. Of the few studies that have considered the impact of the electrodes on $\alpha_{VCC}$, most have focused on interfacial layer oxides (ILOs).

In this work, metals with low enthalpy of oxide formation ($\Delta H_{ox}$), are used to examine the influence of the top electrode interface, in the absence of a significant ILO, on the CV nonlinearity of TaN bottom electrode MIMCAPs with various thickness ALD $HfO_2$ and $Al_2O_3$. If non-linearity is purely a bulk effect then normalizing for $d_{ox}$, one would expect that the *electric field* coefficient of capacitance ($\alpha_{ECC}$) should be independent of $d_{ox}$. Instead, we find that $\alpha_{ECC}$*decreases* with decreasing $d_{ox}$, indicating either an ILO or the direct influence of the interface. A plot of capacitive equivalent thickness vs. optical thickness rules out an ILO. For Au, Ag, Pd, and Ni, $\alpha_{ECC}$ increases with increasing $d_{ox}$, saturating for thick oxides. It has been proposed that for positive $\alpha_{VCC}$ materials ($C_{ox}(V)$ increases with voltage), electrostriction and Maxwell stress lead to a vertical compression of the oxide under applied fields that results in increased capacitance. We further propose that the oxide must expand horizontally to maintain volume. This expansion results in compressive stress in the oxide and tensile stress in the metal, concentrated near the interface. The electrode then serves to inhibit the lateral expansion of the dielectric, reducing overall $\alpha_{ECC}$. Indeed $\alpha_{ECC}$ of 10 nm oxides was found to increase roughly linearly with increased oxide/metal % lattice mismatch. As thinner oxides are used to achieve higher $C_{ox}$, the metal electrodes exert influence over a greater % of the oxide thickness, increasing the electrode importance and its impact on nonlinearity.

New understanding of the impact of electrodes on $\alpha_{ECC}$ should aid in rapid optimization of low $\alpha_{ECC}$ MIMCAPs.

8:20am **TF+EM+MI-WeM2 Difference of the Hysteresis in Capacitance-voltage Characteristics of ALD-$Al_2O_3$ MIS Capacitors on Si and GaN Substrate**, ***Masaya Saito***, *T. Suwa, A. Teramoto,* Tohoku University, Japan, *T. Narita,* Toyota Central R&D Labs. Inc., Japan, *T. Kachi,* Nagoya University, Japan, *R. Kuroda, S. Sugawa*, Tohoku University, Japan

We evaluated the difference of hysteresis in capacitance-voltage(C-V) characteristics of ALD-$Al_2O_3$ MIS capacitors for different semiconductors. N-type Cz-Si and n-type GaN wafers which had the bandgap energies of 1.12 and around 3.4 eV, respectively, were used as semiconductor layers for MIS structures. N-type Si wafer was doped with P of $5\times10^{14}$ $cm^{-3}$. The upper layer (2 μm) of n-type GaN wafer was doped with Si of $5\times10^{16}$ $cm^{-3}$ using a metal-organic vapor phase epitaxy. As the gate insulator layers of the MIS structures, the 10 nm-thick $Al_2O_3$ films were formed by the Atomic Layer Deposition (ALD) using $Al(CH_3)_3$ and $H_2O$ at 75 ºC, followed by the formation of aluminum as the gate electrodes. MIS capacitors were irradiated by the light of white LED to only before the voltage sweeps of C-V measurements at -3 V followed by the voltage sweeps of -3 à 3 V and 3 à -3 V without irradiation.

We observed that the clockwise hysteresis in the case of Si gradually decreased as increasing the time of measurement. On the contrary, the hysteresis in the case of GaN was also clockwise and drastically decreased at the second measurement. It is considered that this difference was caused by the difference of bandgap energies between Si and GaN. In the case of Si, some electrons (holes) injected from Si substrate were trapped to the state near the $Al_2O_3$/Si interface when the positive (negative) bias was applied to gate electrode. When applying the subsequent negative (positive) bias, most of these charges were released because the bandgap energy of Si is small. In the case of GaN, most of these charges trapped to the state near the $Al_2O_3$/GaN interface were not released within the measurement time because of the interface states far from the both band edges owing to the larger bandgap energy of GaN. Therefore, the different hystereses for their MIS capacitors were probably caused by the difference that the trapped charges to the state in the bandgap were released in the case of Si but not released in the case of GaN.

Acknowledgement:

This research is supported by the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan, through its "Program for research and development of next-generation semiconductor to realize energy-saving society. This work was carried out at fluctuation free facility of New Industry Creation Hatchery Center, Tohoku University.

8:40am **TF+EM+MI-WeM3 Monolithic Integration of C-type Erbium Oxide on GaN(0001) by Atomic Layer Deposition**, ***Pei-Yu Chen***, *A. Posadas,* The University of Texas at Austin, *S. Kwon, Q. Wang, M. Kim,* The University of Texas at Dallas, *A. Demkov, J.G. Ekerdt*, The University of Texas at Austin

Motivated by the need for faster device speed, the industry is considering compound semiconductors, such as gallium nitride (GaN) in the III-V family of materials, which have higher electron mobility than silicon. To passivate the nitride surfaces and enable GaN-based electronic devices, a high quality and thermally stable dielectric layer material is required. Recently, rare earth sesquioxides have received attention due to their electrical properties, thermal and chemical stability, and relatively high dielectric constant [1]. Using atomic layer deposition (ALD) with erbium tris(isopropylcyclopentadienyl) [$Er(^iPrCp)_3$] and water, crystalline cubic (C-type) $Er_2O_3$ is successfully grown on GaN at 250 °C for the first time. ALD enables the conformal deposition of $Er_2O_3$ film on GaN and features a stable growth rate of 0.82 Å/cycle in this work. *In-situ* x-ray photoelectron spectroscopy is used to determine film composition and *in-situ* reflection high-energy electron diffraction is used to verify the surface order and the film crystallinity at various stages in the growth process. The cubic structure of $Er_2O_3$ is confirmed by a combination of both out-of-plane and in-plane X-ray diffraction (XRD). The orientation relationships between C-$Er_2O_3$ film and GaN substrate are C-$Er_2O_3$(222) || GaN(0001), C-$Er_2O_3$(-440) || GaN(11-20), and C-$Er_2O_3$(-211) || GaN(1-100). The out-of-plane C-$Er_2O_3$(222) XRD peak shifts as a function of film thickness indicating a slight change in *d*-spacing caused by the presence of strain at the interface as shown in **Fig. 1(a)(b)**. The observed tensile strain results from the lattice mismatch between GaN and $Er_2O_3$. As the film thickness increases, the C-$Er_2O_3$ becomes more relaxed. In-plane XRD also displays peak shifts with opposite trend from the out-of-plane scan as expected. Scanning transmission electron microscopy (STEM) is used to examine the microstructure of C-$Er_2O_3$ and its interface with GaN and is in excellent agreement with the simulated atomic positions (**Fig. 1(c)**). An interfacial layer consisting of 1-3 atomic-layers is observed by STEM. The electron energy loss spectroscopy (EELS) profiles for Ga, Er, O, and N suggest partial oxidization of GaN at the interface. Overall, this work demonstrates a low temperature, all-chemical process for the growth of crystalline C-$Er_2O_3$ on GaN by ALD.

[1] R. Dargis, A. Clark, F. E. Arkun, T. Grinys, R. Tomasiunas, A. O'Hara, and A. A. Demkov, " Monolithic integration of rare-earth oxides and semiconductors for on-silicon technology," *J. Vac. Sci. Technol. A*, 32, 041506 1-8 (**2014**).

9:00am **TF+EM+MI-WeM4 High-Performance p-Type Thin Film Transistors Using Atomic-Layer-Deposited SnO Films**, *S.H. Kim, I.-H. Baek, J.J. Pyeon,* Korea Institute of Science and Technology, Republic of Korea, *T.-M. Chung, J.H. Han,* Korea Research Institute of Chemical Technology, Republic of Korea, ***SeongKeun Kim***, Korea Institute of Science and Technology, Republic of Korea

Since the report of thin film transistors (TFTs) utilizing an amorphous oxide semiconductor of the In–Ga–Zn–O system exhibiting high electron mobility by the Hosono group, considerable efforts have been dedicated to implement these TFTs for emerging applications including flat-panel and flexible displays. Compared with the great progress and success regarding n-type oxide semiconductors, the current status of the development of p-type oxide semiconductors remains far behind.

SnO is a promising p-type oxide with relatively high hole mobility. The low formation energy of Sn vacancies and the more dispersed VBM resulting from hybridization of oxygen 2p and Sn 5s orbitals allow the p-type

conduction of SnO. One critical challenge for high-performance SnO TFTs is the instability of the SnO phase. SnO is less stable than $SnO_2$, indicating the difficulty of growth of SnO.

Here, we demonstrate high-performance p-type TFTs with a single phase SnO channel layer grown by atomic layer deposition (ALD). The performance of the SnO TFTs relies on hole carriers and defects in SnO and near the back-channel surface of SnO as well as the quality of the gate dielectric/SnO interface. The growth of SnO films at a high temperature of 210 °C effectively suppresses the hole carrier concentration, leading to a high on-current/off-current ($I_{on}/I_{off}$) ratio. In addition, the SnO films grown at 210 °C achieve high field effect mobility ($\mu_{FE}$) compared with the SnO films grown at lower temperatures because of their large grain size and lower impurity contents. However, the SnO films grown at 210 °C still contain defects and hole carriers, especially near the back-channel surface. The post-deposition process – back-channel surface passivation with ALD-grown $Al_2O_3$ followed by post-deposition annealing at 250 °C – considerably alleviates the defects and hole carriers, resulting in superior TFT performance ($I_{on}/I_{off}$: $2 \times 10^6$, subthreshold swing: 1.8 $Vdec^{-1}$, $\mu_{FE}$: ~ 1 $cm^2V^{-1}s^{-1}$). We expect that the SnO ALD and subsequent process will provide a new opportunity for producing high-performance p-type oxide TFTs.

9:20am **TF+EM+MI-WeM5 Recent Progresses of Atomic Layer Deposited Oxide Semiconductors for Emerging Display Applications***,* ***Jin-Seong Park****, J. Sheng, J.H. Lee*, Hanyang University, Republic of Korea **INVITED**

Recently, transparent amorphous oxide semiconductors have been widely studied for potential use in flat-panel displays, such as active-matrix organic light emitting diodes or liquid crystal displays. Semiconductors based on indium and zinc oxide compounds have been intensively studied since the report on transparent flexible amorphous InGaZnO TFTs based on physical vapor deposition (Hosono group) in 2004.

Among various thin film deposition methods, Atomic Layer Deposition (ALD) has remarkably developed in semiconductor and nano-structure applications since early 1990. The unique properties, including controlling atomic-level-thickness, manipulating atomic-level-composition control, and depositing impurity-free films uniformly, may accelerate ALD related industries and applications in functional thin film markets. One of big and challenging markets, display industry, has been just started to look at the potential to adopt ALD based films in emerging display applications, such as transparent and flexible displays.

In this talk, I will introduce various oxide semiconductor materials such ZnO, SnOx, InOx, ZnSnO, InZnOx, deposited by ALD processes. InOx and SnOx semiconductors were prepared by using a liquid indium precursor ([1,1,1-trimethyl-N-(trimethylsilyl) silanaminato]-indium) and tin precursor (N, N'-tert-butyl-1,1-dimethylethylenediamine stannylene-tin), respectively. The former exhibited highly transparent conducting oxide film property and the latter did the p-type polarity under a water reactant. The Indium oxide films were grown by ALD using as the metal precursor and hydrogen peroxide ($H_2O_2$) as the oxidant. It is found that the electrical properties of the indium oxide layers strongly depend on the ALD growth temperature. At relatively low growth temperatures below 150 ºC, indium oxide behaves as a transparent semiconducting oxide. Secondly, amorphous indium zinc oxide thin films were deposited at different temperatures. The ALD process of IZO deposition was carried by repeated supercycles, including one cycle of indium oxide and one cycle of zinc oxide. The IZO growth rate deviates from the sum of the respective $In_2O_3$ and ZnO growth rates at ALD growth temperatures of 150, 175, and 200 °C. Thin film transistors were fabricated with the ALD-grown IZO thin films as the active layer. The amorphous IZO TFTs exhibited high mobility of 42.1 $cm^2$ $V^{-1}$ $s^{-1}$ and good positive bias temperature stress stability. Finally, flexible InOx and IZO TFTs on polymer substrates were investigated under various mechanical stress conditions, showing interesting degradations of TFTs. It will be discussed about the following issues.

11:00am **TF+EM+MI-WeM10 Silicon Nitride Thin Films Grown by Hollow Cathode Plasma-Enhanced ALD using a Novel Chlorosilane Precursor***,* ***Xin Meng****, H.S. Kim, A.T. Lucero, J.S. Lee, Y.-C. Byun, J. Kim,* University of Texas at Dallas, *B.K. Hwang, X. Zhou, M. Telgenhoff, J. Young*, Dow Chemical

Plasma-enhanced ALD (PEALD) has become an attractive method of depositing silicon nitride ($SiN_x$) due to its ability to grow high-quality films at low temperatures (≤400°C) for various applications [1]. The use of a chlorosilane precursor, is considered a suitable approach for high-volume manufacturing in the semiconductor industry. Chlorosilane precursors can be applicable to either PEALD $SiN_x$ or thermal ALD $SiN_x$ process. In this work, we have investigated the growth of $SiN_x$ thin films using a novel chlorosilane precursor pentachlorodisilane (PCDS, $HSi_2Cl_5$)(synthesized by Dow Corning Corporation, vapor pressure ~10 mmHg at 20 °C) in comparison with hexachlorodisilane (HCDS, $Si_2Cl_6$). A home-made PEALD system equipped with a hollow cathode plasma source (Meaglow Ltd.) was used in this study.

We analyzed the growth per cycle (GPC) and refractive index (R.I.) as a function of the silicon precursor or plasma exposure time, deposition temperature and plasma power. We also investigated the wet etch rate (WER) in dilute hydrochloric acid as a function of the hydrogen content determined by Fourier Transform Infrared Spectrometry (FTIR), and film density determined by X-ray reflectivity (XRR). Using an $N_2/NH_3$ plasma, saturated growth behavior was demonstrated by PCDS and HCDS with a precursor exposure of ~$3\times10^5$ L. GPC was nearly independent of both deposition temperature and RF power, within the investigated regime. Compared to HCDS, PCDS demonstrated approximately 20–30% higher GPC under the same process condition while maintaining comparable WER.

In addition, it was found that the films with higher hydrogen content had a general tendency to have a higher WER while the films with a higher density or higher R.I. tended to have a lower WER. The oxygen content of the bulk $SiN_x$ films determined by ex-situ X-ray photoelectron spectroscopy (XPS) was approximately 3~5 at. % and didn't have a direct correlation with the WER. Furthermore, MIM capacitors (Al/$SiN_x$/degenerated Si) using PEALD $SiN_x$ films grown with PCDS were fabricated. The capacitors exhibited excellent electrical properties, such as a low leakage current density of $10^{-9}$–$10^{-10}$ A/$cm^2$ at 3 MV/cm, and a high breakdown electric field ~13 MV/cm.

[1]. Meng, X.; Byun, Y.-C.; Kim, H.; Lee, J.; Lucero, A.; Cheng, L.; Kim, J., "Atomic Layer Deposition of Silicon Nitride Thin Films: A Review of Recent Progress, Challenges, and Outlooks," Materials, 9 (12), 1007 (2016)

11:20am **TF+EM+MI-WeM11 Removal of Charge Centers in Hafnia Films by Remote Plasma Nitruration***,* ***Orlando Cortazar-Martínez****, J.A. Torres-Ochoa, C.L. Gomez-Muñoz, A. De Luna-Bugallo, A. Herrera-Gomez*, CINVESTAV-Unidad Queretaro, Mexico

We investigated the effect of soft nitridation on the electrical properties of hafnia-based MOS capacitors. Starting from a cleaned Si (100) wafer a 2 nm of $HfO_2$ thin film is grown by ALD using tetrakis (dimethylamido) hafnium(IV) and water type I as precursors. The growth was performed at a temperature of 250 °C with a 20 sccm flow of ultra-high purity nitrogen (UHP-N). Hafnium oxide soft nitridation was performed by a remote plasma (Litmas) using a power of 2500 W, a substrate temperature of 500 °C, the ultra-high purity nitrogen flow was set at 140 sccm and the working pressure is fixed at $3.5x10^{-2}$ Torr. A 300 nm titanium nitride (TiN) layer is deposited in-situ after nitration in a sputtering system, avoiding undesired contamination. Finally, MOS capacitors were defined using photolitography and etching process.

Capacitance vs voltage measurements characterization was carrying out at different frequencies (1 kHz to 1 MHz). MOS capacitors before nitriding shows a decreasing value in their accumulation capacitance when the frequency is increased. This behavior is attributed to the defects states located inside the oxide layer[1]. In contrast, MOS capacitors measured after nitriding barely shows dispersion in their accumulation regime as the frequency was varied. Also, it can be noted that the threshold voltage remains unchanged.

Films thickness and composition were characterized by ARXPS[2]. The initial thickness and composition were 20.7 Å and $HfO_{2.09}$. After nitridation the thickness changed to 19.8 Å with a composition of $HfO_{1.4}N_{0.48}$. XPS spectra show that the N 1s peak observed at 396.8 eV is associated with the N-Hf bond[3], showing a robust evidence of a substitutional incorporation of nitrogen species into the $HfO_2$ with a saturation process like the one reported in silicon oxide nitridation[4]. Results can be correlated with the soft nitridation process used during fabrication with the remote plasma in which the substitutional nitrogen to oxygen interchange in the $HfO_xN_y$ films keeping the tetrahedral structure from the ALD hafnium as the same as the original but decreasing the amount of the defect states inside the oxide layer.

[1] A. Herrera-Gómez, A. Hegedus, and P.L. Meissner, Appl. Phys. Lett. 81, 1014 (2002).

[2] P.-G. Mani-Gonzalez, M.-O. Vazquez-Lepe, F. Espinosa-Magaña, and A. Herrera-Gomez, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film., vol. 31, no. 1, p. 010601, 2013.

[3] K.-S. Park, K.-H. Baek, D.P. Kim, J.-C. Woo, L.-M. Do, K.-S. No, Appl. Surface Science 257, 1347, 2010.

[4] A. Herrera-Gómez, A. Hegedus, and P.L. Meissner, Appl. Phys. Lett. 81, 1014 (2002).

11:40am **TF+EM+MI-WeM12 Seam-free Bottom-up Filling of Trenches with $HfO_2$ using Low Temperature CVD***,* ***Tushar Talukdar****, W.B. Wang, E. Mohimi, G.S. Girolami, J.R. Abelson*, University of Illinois at Urbana-Champaign

Filling a deep structure is always a transport-reaction problem, one that is sensitive to the geometry of the structure. For example, with parallel sidewalls, a conformal process can mostly fill the structure, but as film

growth diminishes the width of the remaining opening, the AR rises towards infinity; under that condition, no process can eliminate the "seam" in the center. We have shown, using both diffusion and molecular transport models, that a V-shape with an outwards taper (e.g., 3° or more) is needed for conformal coating to work [1]. The other alternative is to develop a process in which film growth is faster at the bottom of the structure: a *superconformal* process in which the growth rate increases progressively with depth. We previously demonstrated a superconformal process for MgO based on (i) a competition for surface adsorption sites between precursor and water co-reactant, and (ii) a large ratio in diffusivity between the high-mass precursor and low-mass water [2].

Here, we attempt to develop superconformal growth of $HfO_2$ from tetrakis dimethylamido hafnium (TDMA-Hf) based on our previous method for MgO. We choose the TDMA-Hf precursor because it affords excellent film quality in ALD, e.g., $HfO_2$ for gate dielectrics. However, the reaction kinetics of this precursor with water as the co-reactant differ strongly from the competitive adsorption model that is the basis for superconformal MgO deposition. Instead, the film growth rate is nearly independent of precursor flux and increases almost linearly with water flux.

For $HfO_2$, we therefore introduce a new approach in which water is injected in a forward-directed flux through a tube aligned with the trench axis. Water is transported ballistically to the trench bottom, where it partially reflects and creates a *virtual source at the trench bottom*. At the same time, the coating conditions are nearly conformal. The combination of a virtual source at the bottom and nearly conformal growth affords a V-shaped profile and excellent filling characteristics. We also introduce a simple kinetic model that predicts the fill profile based on the measured growth rate kinetics.

A limitation to this method is that rapid film growth also occurs on the exposed top surfaces. For a structure with parallel sidewalls, this tends to narrow the opening such that pinch-off can occur prior to complete fill. One solution is to use a structure with an outwards taper to the sidewalls. Another potential solution is to suppress growth at the trench opening using an inhibitor, which we will demonstrate.

1. W. B. Wang and J. R. Abelson, JAP **116**, 194508 (2014)

2. W. B. Wang *et al.*, JVST A **32**, 051512 (2014)

12:00pm **TF+EM+MI-WeM13 Low-κ Organosilicon Thin Films Deposited by iCVD for Electrical Insulation of Through Silicon Vias**,
***Mélanie Lagrange***, *C. Ratin, M. Van-Straaten, C. Ribière, T. Mourier, V. Jousseaume*, CEA-Leti, France

3D integration is considered as an attractive technological route to fabricate cost-effective, high-performance products with reduced size.[1] This technology is based on the use of Through Silicon Vias (TSV), which are vertical connections between electronic components. One of the key steps in TSV fabrication is their electrical insulation from the Si substrate. Depending on the TSV integration scheme used, the allowed thermal budget is limited. For instance, via-middle and via-last integrations need process temperatures lower than 400°C and 200°C, respectively. Moreover, considering the high Aspect Ratio (AR ≥ 10) required by the TSV-middle integration, a highly conformal deposition technique is needed.

Initiated Chemical Vapor Deposition, iCVD, is a low-energy and solvent-free polymer film fabrication process. It is able to deposit solid materials with high step coverage of deep blind features on low-temperature substrates. In the last decade, this versatile method has enabled the deposition of numerous types of polymers, including organosilicons (OSi)[2]. OSi polymers are low-κ materials having shown to be useful in a broad range of applications, including insulation layers in electronic devices.[3]

In this study, dielectric thin films were deposited from vinyl-based OSi precursors using iCVD. The impact of different process conditions on deposition rate, chemical composition and electrical properties of the films have been investigated. Thin films deposited at low temperature, typically < 60°C, can present low dielectric constants (< 3) without the need of any post-deposition treatment. However the films have to face 400°C thermal budget from BEOL process in via-middle integration, therefore a need for sample stabilization emerged. The impact of thermal or UV-assisted annealing on the films properties was investigated in order to understand the thermal stability of the materials and extrapolate their behavior during TSV fabrication and its integration in a full device fabrication flow (BEOL and Back side process). A study of the step coverage achieved by iCVD-deposited thin films in 10*100 µm TSV was performed. It shows that iCVD is promising to deposit materials with high conformity in high AR TSV. Finally, the integration of these OSi polymers in functional TSV, using a standard metallization process on 300 mm wafers, is presented.

The OSi films depositions were processed in a vertical flow reactor, under a collaboration with Kazuya Ichiki, Bruce Altemus and Jacques Faguet, at TEL Technology Center, America.

[1] Gambino et al., *Micro. Eng.* **135** (2015)

[2] Wang et al., *Adv. Mater.* (2017)

[3] Chen et al., *Annu. Rev. Chem. Biomol. Eng.* **7** (2016)

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