Thin Film
Room 105A - Session TF+EM+MI-WeA

Thin Films for Microelectronics

Moderators: Paul Poodt, Holst Centre / TNO, Netherlands, Christophe Vallee, LTM, Univ. Grenoble Alpes, CEA-LETI, France

2:20pm **TF+EM+MI-WeA1 Impact of ALD VO_2 Film Thickness on the Electrical and Optical Properties of the Metal-Insulator Phase Transition**, ***Virginia Wheeler***, *B.P. Downey, J. Roussos, M. Currie, A. Giles, C. Ellis, J. Tischler, J. Caldwell, D.J. Meyer, C.R. Eddy, Jr.,* U.S. Naval Research Laboratory

VO_2 films are known to undergo a metal-insulator phase transition (MIT) at a critical temperature (T_c = 68°C) near room temperature which results in significant changes in thermal emittance, optical transmittance and reflectance, and intrinsic electrical properties; thus attracting interest in a variety of new electronic, optoelectronic, and photonic applications. Atomic layer deposition (ALD) provides a way to obtain large area film uniformity, abrupt interfaces and angstrom-scale control of thickness conformally across planar, as well as three-dimensional, high surface area nanostructures, which could be used to integrate VO_2 films into complex electronic and optical devices for additional functionality. In this work, VO_2 electrical devices and VO_2 coated SiC-based nanoresonantors are used to investigate the impact of film thickness on electrical and optical properties.

The influence of VO_2 thickness on electrical performance was investigated using a simple two-terminal device structure. Sheet resistance measurements as a function of temperature revealed that the R_{off}/R_{on} ratio increased with increasing VO_2 thickness, up to R_{off}/R_{on} of ~7000 for a 92 nm film. Similarly, the T_c increased slightly with increasing thickness (T_c = 66°C for 35nm, 73°C for 92nm), while all films show relatively low hysteresis (ΔT<8°C). Initial small-signal rf measurements using the 92 nm ALD VO_2 film demonstrated a cut-off frequency of greater than 1 THz, indicating the potential for rf-switch applications into millimeter wavelength frequencies using these ultra-thin ALD films, and the potential of these films to be conformally integrated into complex circuits with an ALD process.

For applications in the infrared, surface phonon-polariton-based SiC nanoresonators exhibiting strong, narrowband absorption features within the 10-12.5 μm range were coated with different thickness ALD VO_2 films. Since these films are transparent to infrared light below the Tc and reflective above the Tc, conformally coating these SiC nanostructures provides a way to add functionality to these structures by modulating the amplitude of the resonances with temperature. Initial results show that the magnitude of the resonance suppression increases with increasing VO_2 thickness and a VO_2 film thickness greater than 16nm is required to fully inhibit the signal. It was also determined that the SiC resonances become increasingly shifted and broadened with increasing thickness of the VO_2 coating. These results suggest that VO_2 can add active tunability and integrated switching to optical structures.

2:40pm **TF+EM+MI-WeA2 Study of Ru Silicidation with and without Sub-nm ALD TiN and TaN Barrier/nucleation Layers for Ru Interconnect Applications**, ***Sonal Dey***, SUNY College of Nanoscale Science and Engineering*; K.-H. Yu, S. Consiglio, K. Tapily, C.S. Wajda, G.J. Leusink,* TEL Technology Center, America, LLC*; J. Jordan-Sweet, C. Lavoie,* IBM T.J. Watson Research Center*; A.C. Diebold,* SUNY College of Nanoscale Science and Engineering

With continual shrinkage of the feature size in devices, contribution of the Cu interconnects, liners, and barrier layers to the RC time-delay is becoming a significant obstacle at the 10 nm technology node and below. Ru is a potential candidate to replace Cu as an interconnect material for ultra-scaled line widths where scaling effects on Cu line resistance become increasingly problematic. Ru has already been demonstrated to be useful as the seed layer for Cu electroplating but has been shown to be an inadequate barrier to prevent Cu diffusion into surrounding BEOL dielectrics and requires the use of an additional barrier layer such as a Ta-based nitride. In addition, TaN deposited by PVD is reaching a limit in its ability to conformally coat aggressively scaled structures in the sub 10 nm node. Accordingly, in this study we evaluated the thermal stability of thin Ru films (3 nm) with and without ultra-thin (~0.5 nm) highly conformal ALD TiN and TaN films as nucleation and/or barrier layers for Ru interconnect applications in advanced technology nodes. Si (100) substrates were chemically cleaned to remove the native oxides followed by deposition of ultra-thin ALD TiN and TaN barrier films. $TiCl_4$ and $Ta(NCMe_3)(NEtMe)_3$ precursors, along with NH_3, were used for deposition of the TiN and TaN layers, respectively. Using $Ru_3(CO)_{12}$, 3 nm of Ru was deposited by CVD on top of these refractory metal nitride films and also directly on Si. We also used PVD Cu (25nm)/Si as a control stack for our experiments. The diffusion kinetics of metal-silicide formation was evaluated using in-situ rapid thermal anneal (RTA) synchrotron x-ray diffraction (XRD) measurements and a Kissinger-like analysis to determine the transition temperatures of the metal-silicidation in these stacks and the effective activation energy (E_a) using three different ramp rates (0.3, 3, and 10 °C/s). The Ru/Si stack showed higher E_a = 2.48 eV as compared to the Cu/Si stack (E_a = 1.88 eV). A 0.5 nm thick TaN (E_a = 2.88 eV) was found to act as a more effective barrier as compared to 0.5 nm thick TiN (E_a = 2.64 eV). Scanning electron microscopy (SEM) data shows that both TaN and TiN act as nucleation layers for the growth of Ru microstructure on top. A fewer number of pin holes was observed for Ru films deposited on TaN although there was not significant change on the wettability properties of the Ru film with either TiN and TaN nucleation layers underneath. Additional physical and chemical characterization with XPS and TOF SIMS were also performed to gain understanding of the film stack properties before and after silicide formation.

3:00pm **TF+EM+MI-WeA3 2D - Material and Process Challenges of the Ultimate Thin Films in Nanoelectronics**, ***Stefan de Gendt***, KU Leuven, IMEC, Belgium*; S. Brems, D. Chiape,* IMEC, Belgium*; M. Heyne, K. Verguts,* KU Leuven, IMEC, Belgium*; R. Philipson,* KU Leuven, Belgium*; C. Lockhart de la Rosa, A. Delabie,* KU Leuven, IMEC, Belgium*; S. De Feyter,* KU Leuven, Belgium*; C. Huyghebaert,* IMEC, Belgium **INVITED**

Graphene has emerged as one of the promising candidates for post-Si electronics, both for channel (Logic, RF, sensors) and interconnect applications. Further, other two-dimensional (2D) materials such as transition metal dichalcogenides (MX2, with M a transition metal of group 4–7 and X a chalcogen) have versatile properties that complement or even supersede those of graphene. Both categories however share similar problems, related to the absence of good quality synthesis processes, subsequent layer transfer processes and doping and contacting challenges. To tackle the **first challenge** – growth – chemical vapor deposition (CVD) is widely considered to be the most economically viable method to produce both graphene and MX2 materials for high-end applications. However, in most cases, this deposition technique typically yields undesired grain boundaries in the 2D crystals, which drastically increases the sheet resistance of the layer. Strategies w.r.t. template and process development will be presented. Further, given growth temperature and template, direct growth on devices is often unfeasible, thus a **second challenge** relates to the requirement for a transfer process. For graphene, several transfer process possibilities have been evaluated, but up to now, the graphene transfer suffers from contamination often coming from the temporary support layer and/or etching products, wrinkle formation during bonding, crack formation during graphene handling, ... Moreover, with improvement in 2D quality the release from the growth template is hindered due to increased adhesion forces. At least for MX2 materials, the transfer challenge can be avoided through area selective growth. A process based on a reductive two step CVD process will be presented, whereby in a first step the metal precursor (WF6) is reduced to a lower oxidation state through sacrificial reaction with Si. Subsequently, the metallic film is allowed to react with a sulphur precursor (H2S). Challenges are again related to the (poly)crystallinity of the films and the control of lateral 2D versus crystal 3D growth. Last but not least, a **third challenge** related to 2D materials resides in the contacting and doping of these materials. Different strategies have been proposed to achieve doping, but in this presentation we will demonstrate the self-assembly of organic molecules physisorbed on top bulk and thin 2D layers as a means to achieve controlled doping.

4:40pm **TF+EM+MI-WeA8 Atomic Layer Deposition of Stoichiometric $TaSi_2$ on Si(001)**, ***JongYoun Choi***, *S.W. Park,* University of California San Diego*; R. Hung,* Applied Materials Inc.

Transition metal disilicides are of great interest in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) due to their ability to tune the work function at the metal contact in the source/drain regions. Various kinds of transition metal silicides such as $TiSi_2$, $NiSi_2$ and WSi_2 have been studied in previous decades, however, nanoscale studies of $TaSi_2$ are relatively scarce. Previously, Lemonds *et al.* successfully demonstrated atomic layer deposition (ALD) of tantalum silicide ($TaSi_x$) on SiO_2 using TaF_5 and Si_2H_6. In this work, it is demonstrated that using similar reaction conditions $TaSi_2$ can be grown by ALD process on oxide-free clean Si(001). The growth rate of $TaSi_2$ on Si(001) was monitored *in-situ* using a Quartz Crystal Microbalance (QCM) during the deposition. This enabled

optimization of the TaF_5 and Si_2H_6 dosing to avoid chemical vapor deposition (CVD) components. Scanning tunneling microscopy (STM), X-ray photoelectron spectroscopy (XPS), scanning tunneling spectroscopy (STS) and atomic force microscopy (AFM) have been used to investigate the atomic and electronic structure of Si(001) surface after $TaSi_2$ thin film deposition. HF cleaned Si(001) was used for the substrate. The chemical composition was determined by XPS after ALD to be that of a stoichiometric $TaSi_2$ film formed on the Si substrate. The key variables in forming stoichiometric $TaSi_2$ are the ratio of the precursors and the surface temperatures. In the ALD process, a 100x fold excess of Si_2H_6 is required to prevent formation of TaOx; in addition, the surface temperature must be above 240C. These requirements for excess Si_2H_6 and a high surface temperature are likely due to high activation barrier to break the residual Ta-F bonds on the surface after the TaF_4 half pulse since the Ta-F bonds are stronger than the Si-H bonds.

5:00pm **TF+EM+MI-WeA9 Different Approaches for Enhancing the Thermal Stability of $Ge_2Sb_2Te_5$ Thin Films by Carbon Addition**, ***David Adams**, K. Childs, T. Gurrieri, W. Rice,* Sandia National Laboratories

Different forms of carbon-doped $Ge_2Sb_2Te_5$ chalcogenide thin films have been evaluated for potential use in phase change memory and thermal sensor applications. This includes films sputter deposited from single, carbon-doped targets and refined multilayers made by sequential deposition of chalcogenideand C layers. In both forms, the crystallization temperature (T_{cryt}) and the resistance change through crystallization vary with carbon content. Doped chalcogenide films sputter deposited from single targets exhibit increased T_{cryt} as the concentration of C is made larger. For example, films having ~7 at.% C exhibit a T_{cryt} that is approximately one hundred and fifteen degrees above that of undoped $Ge_2Sb_2Te_5$. Films with reduced C content, in the range 1-6 at.%, show intermediate crystallization temperatures. Multilayers fabricated by the sequential deposition of thin chalcogenideand C layers behave much like films grown from single targets, provided that multilayer periodicity is made small, < 3 nm. The crystallization temperature of multilayers also increases with C concentration and a prompt transition to a crystalline phase is observed when the carbon content is low. Interestingly, multilayers made with $\geq$ 9 at.% C do not transition abruptly to a crystalline state. Instead, a transformation occurs over a broad range of elevated temperature. Each form of chalcogenide thin film exhibits a decreased resistivity upon crystallization. In most cases, resistivity is reduced by 5 decades upon transforming to a face centered cubic structure or a subsequent hexagonal close packed lattice at higher temperature. The changes to microstructure and thickness associated with phase change will also be described. These film properties are investigated by cross-section and plan view electron microscopy.

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5:20pm **TF+EM+MI-WeA10 Comparison of Electromigration and Resistivity in On-chip Co and Cu Damascene Nanowires**, ***C.-K. Hu**, J. Kelly, J.H-C. Chen, H. Huang, Y. Ostrovski, R. Patlolla, B. Peethala, P. Adusumilli, T. Spooner,* IBM Research Division, Albany*; L. Gignac, S. Cohen,* IBM Research Division, T.J. Watson Research Center*; R. Long, G. Hornicek, T. Kane, G. Lian, M. Ali,* IBM Systems*; V.M. Kamineni, F. Mont, S. Siddiqui,* GLOBALFOUNDRIES

Cu metallization has been used for back end of the line (BEOL) on-chip interconnections since 1997. However, scaling Cu BEOL dimensions has increased Cu resistivity and degraded electromigration (EM) reliability. The Cu effective resistance has increased rapidly as the interconnect size has reduced and the ratio of liner area to total interconnect cross sectional area has increased. This size effect was caused primarily by increasing the probability of electron scattering with interfaces and grain boundaries. The EM lifetime degradation was caused by an increase in the volume fractions of diffusing atoms at interfaces and grain boundaries and a decrease in the void volume required to cause EM failure. It is estimated that ~ 70% of interconnect metal area could be occupied by the liner in the 5 nm technology node for reliable Cu metallization. To this end, an alternate metal, Co, was investigated. Multi-level Co BEOL was fabricated using typical 10 nm node technology wafer processing steps. A Co dual damascene process was used to fill the interconnect trenches and holes. The present Co resistivity study showed a similar size effect in Co as in Cu. This can be explained by the fact that the slope of resistivity vs. interconnect size is proportional to the product of the electron mean free path and resistivity, with the two slopes being about the same for Cu and Co. The effective resistivity difference between Co and Cu becomes small when no liner is used in Co lines. EM in 22 nm to 88 nm wide Co lines was tested using sample temperatures from 376°C to 425°C. Two–level EM structures consisted of either Co M1 to Co V1 to Co M2 or W CA to Co V0 to Co M1. The EM stress conditions for Co were far more severe than those for Cu. For comparison, EM in 24 nm wide Cu lines with a Co cap was also included. These data showed that both Co and Cu BEOL were highly reliable EM.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities

5:40pm **TF+EM+MI-WeA11 UV/VUV Curing Process for Low-k Organosilicate Dielectrics**, ***Huifeng Zheng**, X. Guo, D. Pei, W. Li, J. Blatz, K. Hsu, D. Benjamin,* University of Wisconsin-Madison*; Y. Lin, H. Fung, C. Chen,* National Synchrotron Radiation Research Center, Taiwan, Republic of China*; Y. Nishi,* Stanford University*; J.L. Shohet,* University of Wisconsin-Madison

Porous SiCOH films are of great interest in semiconductor fabrication due to their low-k properties. Post-deposition treatments of SiCOH thin films are required to decompose labile pore generators (porogens) and to ensure optimum network formation to improve the electrical and mechanical properties of low-k dielectrics. The goal of this work is to optimize the vacuum-ultraviolet spectrum to identify those wavelengths that will have the most beneficial effect on improving dielectric properties and minimizing damage without the need for thermal heating of the dielectric. Vacuum ultraviolet (VUV) irradiation between 8.3-8.9 eV was found to increase the hardness and elastic modulus of low-k dielectrics at room temperature. Combined with UV exposure of 6.2 eV, it was found that this UV/VUV curing process compares favorably with current UV curing. The results also show that UV/VUV curing can overcome many of the drawbacks of UV curing and improve properties of dielectrics more efficiently without the need for high-temperature heating of the dielectric.

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6:00pm **TF+EM+MI-WeA12 Effects of Cesium Ion Implantation on the Mechanical and Electrical Properties of Organosilicate Low-k Films**, ***Weiyi Li**, D. Pei, X. Guo, M.-K. Cheng, S. Lee,* University of Wisconsin-Madison*; Q. Lin,* IBM Research Division, T.J. Watson Research Center*; S.W. King,* Intel Corporation*; J.L. Shohet,* University of Wisconsin-Madison

The effects of cesium (Cs) ion-implantation on uncured plasm a-enhanced chemical-vapor-deposited (PECVD) organosilicate low dielectric constant (low-k) (SiCOH) films have been investigated and compared with the effects of ultraviolet (UV) curing. The mechanical properties, including the elastic modulus and hardness, of the films were improved by up to 30% with Cs implantation, and further up to 52% after annealing at 400°C in a N2 ambient for one hour. These improvements in mechanical properties are either comparable with or better than the effects of UV-curing. These improvements are attributed to an enhancement of the Si-O-Si network structure. The k-value of the SiCOH films increased slightly after Cs implantation, and increased further after annealing. These increases are attributed to two carbon-loss mechanisms, i.e. the carbon loss due to Si-CH3 bond breakage from implanted Cs ions, and the carbon loss due to oxidation during the annealing. The time-zero dielectric breakdown strength was improved after the Cs implantation and the subsequent annealing, and were shown to be better compared with the UV-cured SiCOH films. Within the investigated range of implantation dose, an optimal dose can be found to achieve the best effects. These results indicate that Cs ion implantation has the potential to be a supplement to or a substitution for the incumbent UV curing method for processing SiCOH low-k films.

This work was supported by the Semiconductor Research Corporation under Contract 2012-KJ-2359.

[1] Y. Kayaba, K. Kohmura, H. Tanaka, Y. Seino, T. Odaira, F. Nishiyama, et al., "Electrical reliabilities of highly cross-linked porous silica film with cesium doping," Journal of the Electrochemical Society, **155**, G258 (2008)

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