Plasma Science and Technology
Room 104B - Session PS-MoM

Advanced FEOL/Gate Etching

Moderator: Ankur Agarwal, Applied Materials, Inc.

8:20am **PS-MoM1 Novel Etch Strategies for Sidewall Image Transfer**, ***Sonam Sherpa***, *P. Chan, A. Ranjan,* Tokyo Electron Ltd.

Sidewall image transfer (SIT) is an indirect patterning method that involves the deposition and etching of silicon nitride spacer to achieve sub-lithographic linewidths. Current approaches to etch silicon nitride spacer face two main challenges --— footing and corner rounding. Solution to these problems requires a non-polymerizing chemistry that must be anisotropic and yet avoids the adverse impact of ion-bombardment. To this end, an alternative etching process based on the modification of silicon nitride by light ions followed by the selective removal of the modified layers by DHF has already been reported [1]. However, this process uses non-compatible etch techniques (dry and wet etch). To overcome this challenge, we have developed a plasma-based alternative to DHF. After the spacer etch, isotropic etching of silicon with infinite selectivity to the nitride spacer and underlying oxide is required for mandrel pull. Current methods used to etch silicon involve the redeposition of etch by-products and bombardment by energetic ions. Therefore, these processes are not isotropic and result in footing and significant damage to the underlying material.

In this presentation, we will demonstrate the feasibility of our approach to etch silicon nitride spacer without any footing and corner rounding. In addition, damage to the underlying oxide is negligible. We will also discuss the effects of non-idealities such as scattering and deflection of ions during the hydrogen plasma treatment and the incoming topographical defect on the etch profile. In addition, we will demonstrate the feasibility of novel strategies for isotropic etching of silicon with infinite selectivity to oxide, nitride, and other materials. These processes are by-product free and we do observe any footing. In addition, damage to the underlying material is negligible.

1. N. Posseme,O. Pollet, and S. Barnola, Appl. Phys. Lett., **105**, 051605 (2014).

8:40am **PS-MoM2 Enhancing Fin Retention in Low-K Spacer Etch Processes Using a Highly Selective Etch Chemistry**, *N.P. Marchack,* IBM Research Division, T.J. Watson Research Center*; E. Miller,* IBM Research at Albany Nanotech*; R.L. Bruce, H. Miyazoe, E.M. Sikorski,* ***Sebastian Engelmann****, E.A. Joseph,* IBM Research Division, T.J. Watson Research Center*; S. Kanakasabapathy,* IBM Research at Albany Nanotech

Low-k spacer materials such as SiBCN have garnered attention recently for advanced technology nodes due to their controllable electrical conductivity, low thermal expansion coefficient and potential for reducing loading capacitance. [1] Of particular concern in a spacer etch process is reducing the damage caused to materials such as the bottom oxide (BOX) and the underlying fins in FinFET systems. This is often a difficult challenge owing to the tight pitches and widely disparate critical dimensions (CDs) between the fin and gate geometries.

We present a spacer etch process using a novel high-selectivity gas chemistry that shows minimal damage in a FinFET system with SiBCN spacer deposited over SiGe fins. In addition to reduced damage compared to a conventional CH_3F/O_2 plasma chemistry, we also demonstrate greatly improved throughput even at low duty cycles by taking advantage of the unique chemical properties of the gas. We show <5nm SiGe fin loss for long overetch values, with minimal box loss as measured by high-resolution transmission electron microscopy (TEM).

The effect of pulsed plasma parameters are analyzed via optical emission spectroscopy (OES) in an attempt to define the etching mechanisms, as well as explain the difference between blanket etch conditions and patterned features. We focus on the effect of He dilution within the plasma as well as the effect of phase difference between source and bias for synchronous pulsing cases.

References:

[1] R.G. Southwick et al., IEEE International Reliability Physics Symposium pp. BD.2.1-2.4, 2014

9:00am **PS-MoM3 Effect of the Amount of Hydrogen During SiN etching on Etching Properties**, ***Nobuyuki Kuboi****, H. Minari, M. Fukasawa, Y. Zaizen, J. Komachi, T. Kawamura, T. Tatsumi,* Sony Corporation, Japan

Silicon nitride (SiN) is an essential film in complementary metal oxide semiconductor devices. The amount of hydrogen contained in SiN films depends on the process conditions used in chemical vapor deposition (CVD), and strongly affects the etching properties of etching rate (*ER*), C-F polymer thickness ($T_{C\text{-}F}$), and damage. Therefore, revealing the mechanism of how hydrogen influences etching is very important to predict and control damage distribution considering the etching profile, and to develop etching processes with high selectivity for SiN over SiO_2.

To model SiN etching under the effect of hydrogen, we performed experiments using a dual-frequency capacitively coupled plasma system. We prepared three kinds of SiN_x:H_y films with y = 2.6%, 16.8%, and 21.9% (denoted as LP-SiN, Low-H SiN, and High-H SiN, respectively) on Si substrates using different CVD processes. The films were treated with CH_2F_2/O_2/Ar plasma under a gas pressure of 20 mTorr and Vpp of 350 V, for which we measured *ER* and $T_{C\text{-}F}$ values. We also measured plasma and surface conditions using various monitoring techniques. We analyzed the results through a first-principles calculation with VASP [1].

We found that for the low $CH_2F_2/(CH_2F_2+O_2)$ ratio where few C-F polymer layers existed, the *ER* values of High-H SiN were 20%–40% smaller than those of LP-SiN and Low-H SiN. In contract, inverse behavior was observed in the case of a high $CH_2F_2/(CH_2F_2+O_2)$ ratio. Considering variation of OES data and reactivity estimated by the VASP calculation, under the assumption that the etching front consisted of two layers (C-F polymer layer and reactive layer) [2], not only reaction between the outflux of H from the reactive layer and F from plasma but also termination of Si dangling bonds by H seems to cause variation of the *ER* value when the $CH_2F_2/(CH_2F_2+O_2)$ ratio is low. Because a C-F polymer layer of moderate thickness existed over the reactive layer at high $CH_2F_2/(CH_2F_2+O_2)$ ratio, some H was consumed by reaction with C in the polymer layer, which weakened the effects of H such as deactivation of F and termination of Si dangling bonds. This seems to lead to the inverse behavior observed at high $CH_2F_2/(CH_2F_2+O_2)$ ratio.

We formulate the above effect of H and include it in our SiN surface reaction model using the 3D voxel-slab method [3], reproducing *ER* and $T_{C\text{-}F}$ values. We also demonstrate SiN side-wall etching of fin-type field-effect transistors and discuss how to control etching profile and damage distribution.

[1] G. Kresse and J. Furthmüller, Phys. Rev. B **54**, 11169 (1996).

[2] M. Matsui *et al*., J. Vac. Sci. Technol. A **19**, 2089 (2001).

[3] N. Kuboi *et al*., J. Vac. Sci. Technol. A **33**, 061308 (2015).

9:20am **PS-MoM4 Dual Channel Si/SiGe Fin patterning for 10nm Node and Beyond**, ***Fee Li Lie****, E. Miller, P. Xu, S. Sieg, M. Sankarapandian,* IBM Research*; S. Schmitz, P. Friddle,* Lam Research Corporation*; G. Karve, J. Strane,* IBM Research*; K.Y. Lim, K. Akarvardar, M.G. Sung,* GLOBALFOUNDRIES, Inc.*; S. Kanakabasapathy,* IBM Research

As geometric scaling of silicon CMOS technology reaches its limits, continued device performance enhancement requires innovative approaches such as alternative channel materials. Owing to its relatively high hole mobility, much attention has been given to SiGe as a candidate for PFET channel material. The introduction of Ge in the material system affects the vertical and lateral etch behavior of the system depending on the Ge%. Typical balancing act of sidewall passivation and etch to yield vertical and on-target critical dimension (CD) fins now needs to be done on both Si and SiGe simultaneously. Furthermore, subsequent dry/wet clean processes, which generally does not impact Si fins, also interacts with SiGe fin and affects the final fin profile and CD. In this paper, we will present key challenges and approaches pertaining to etching dual channel Si/SiGe fin and subsequent dry/wet clean processes.

9:40am **PS-MoM5 Computational Patterning and Process Emulation: Linchpins to Enable Continued Scaling through Design Technology Co-optimization for Advanced Nodes**, ***Derren Dunn****,* IBM Corporation **INVITED**

Enabling continued scaling at a pace that meets market demands will require new paradigms to define and evaluate early hardware design guidelines. Increasingly, patterning process implementations will be key

factors in defining the boundaries of design spaces available for nodes beyond 10 nm. Self aligned patterning approaches will enable design spaces with significantly different entitlements than direct print patterning strategies due to process control dependencies, complexity, and physical process limitations. Identifying early design guidelines through process simulation and emulation that incorporate a full range of patterning processes required for a given front end of line (FEOL) approach will be key to delivering nodes on time. These processes will undoubtedly include lithography, reactive ion etch, spacer deposition, and wet clean processes. In addition, EUV solutions will require accurate estimates of line width variation, line end pull-back, and new materials challenges that will influence early design decisions. In this talk, we will demonstrate how coupling advanced process simulation with process emulation can be used to evaluate early FEOL design guidelines and establish criteria for equipment and materials vendors. We will also suggest approaches to establishing design entitlement metrics for typical FEOL self aligned patterning processes and EUV direct print approaches that might be used in future gate and fin process modules.

10:40am **PS-MoM8 Overcoming Challenges of sub-10NM FinFET Gate Etching in Halogenated Plasmas.** ***Sergey Voronin,*** TEL Technology Center, America, LLC*; J.R. Sporre, S. Kanakasabapathy,* International Business Machines – Research Division*; A. Ranjan,* TEL Technology Center, America, LLC

Moore's law extension in the semiconductor industry requires processing of features at nanometer scale. Approaching sub-10NM technological fabrication we face more stringent requirements to the etch process (high anisotropy and high selectivity to the mask films).

We present peculiarities and new challenges of 3D gate etch processing in halogen-based plasmas. These include by-product -free etching of narrow features, "FIN-Gate" corner residue removal, prevention of merging of the neighboring gates and advanced selectivity control to the FIN oxide. To combine all these in one process, we need multiple unique steps responsible for certain stages of etching. The etching mechanisms and dependence of the etching properties (selectivity, anisotropy and etch rate) on the plasma discharge parameters (electron temperature, ion and radical densities, ion energy) will be described for each step. We have successfully approached the 7NM technological node at aspect ratios and, etch depths up to 6:1 and 160 nm, respectively, with a potential for the next technological generation.

An additional subject of discussion is related to surface-plasma interactions between charged and neutral species in HBr plasmas. Formation and deposition of non-volatile bromine-containing by-products $SiBr_x$ (x=1,2) and $SiBr_xO_y$ can result in clogging of narrow features, etch profile distortion, limited etching depth and residual Si at high aspect ratios. These non-volatile species are accumulated on the process chamber wall, desorb to the gas phase and can re-deposit on the processed wafer for long times – well after the main etch process is over. We demonstrate the importance of the chamber wall chemistry condition and plasma discharge parameters in formation and re-deposition of these species. Chamber wall surface cleaning by fluorine-containing plasmas and lowering the source power resulted in significantly smaller amounts of by-product and can be used as profile control knobs in the process.

11:00am **PS-MoM9 Gate Etch Challenges Introduced by FinFET Gate Pitch Scaling*****, John Sporre,*** IBM Research Division*; X. Liu,* IBM Research Division, T.J. Watson Research Center*; S. Seo,* IBM Research Division*; C. Prindle,* GLOBALFOUNDRIES, Inc.*; P. Montanini,* IBM Research Division*; R. Xie,* GLOBALFOUNDRIES, Inc.*; M. Sankarapandian, S. Mehta, M. Breton, S. McDermott, S. Kanakasabapathy,* IBM Research Division*; B. Haran,* IBM Research

Continued scaling of FinFET technology introduces unique challenges with respect to patterning high aspect ratio structures. In addition to the traditional challenge of etching a gate with uniform sidewall and cross wafer uniformity, new challenges are introduced as a result of the reduction of inter-gate spacing. Maintaining selectivity to dielectrics during Si etch can result in profile degradation due to etch polymer by-product pinch-off. Low polymer producing chemistries can prevent this pinch-off, but with the cost of unacceptable Fin erosion. Furthermore, gate profile and pitch control can have significant impact on down stream process stability and may result in downstream gate bending. In this paper, the unique challenges caused by gate pitch scaling will be explored with respect to not only their impact on downstream functionality, but also to the gate etch itself.

11:20am **PS-MoM10 Hybrid Fin reveal for tight Fin Pitch Technologies*****, Peng Xu,*** IBM Research Division*; P. Wang,* Lam Research Corporation*; Z.X. Bi,* IBM Semiconductor Technology Research*; T. Devarajan,* IBM Research Division*; B. Nagabhirava, A. Basavalingappa,* Lam Research Corporation*; F.L. Lie, J. Strane, M. Sankarapandian, S. Mehta, R. Conti,* IBM Research Division*; M. Goss,* LAM Research Corporation*; D. Canaperi, D. Guo, S. Kanakasabapathy,* IBM Research Division

FinFET based CMOS technologies continue scaling down in Fin Pitch1-3. Self-aligned double patterning (SADP) and Self-aligned quadruple patterning (SAQP) have been used to form tight Fin pitch structure. Device requirements and layout constraints can result in the need to cut different numbers of fins, which form variable spaces between fins, but a consistent Fin height must be maintained. In addition to the space variability, gap fill oxide density variations are observed depending on local feature density. A key process for defining the height of the active fin for Bulk Substrates is the Fin reveal process

Such space and film density variations between Fins introduce significant challenges for the Fin reveal process, especially in the sub 40nm Fin pitch range. In this paper, we show initial results from a hybrid Fin reveal process, that combines anisotropic etching with reactive clean techniques. We show the ability to maintain fin reveal depth uniform across feature densities and quality.

1.Chang *et al.*, "Extremely scaled silicon nano-CMOS devices," in *Proceedings of the IEEE*, vol. 91, no. 11, pp. 1860-1873, Nov 2003.

2.K. I. Seo *et al.*, "A 10nm platform technology for low power and high performance application featuring FINFET devices with multi workfunction gate stack on bulk and SOI," *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*, Honolulu, HI, 2014, pp. 1-2. Saurabh Sinha, Greg Yeric, Vikas Chandra, Brian Cline, and Yu Cao. 2012. Exploring sub-20nm FinFET design with predictive technology models. In *Proceedings of the 49th Annual Design Automation Conference* (DAC '12). ACM, New York, NY, USA, 283-288.

11:40am **PS-MoM11 Damage Free Plasma Etching Processes for the Patterning of InGaAs fin for the sub-10nm Technological Node*****, Maxime Bizouerne,*** *E. Pargon,* LTM, Univ. Grenoble Alpes, CEA-LETI, France*; P. Burtin,* CEA, LETI, MINATEC Campus, France*; C. Petit-Etienne, E. Latu-Romain, S. Labau, M. Martin,* LTM, Univ. Grenoble Alpes, CEA-LETI, France

The conventional Si CMOS technology recently encounters difficulties to maintain its dimensional scaling owing to the high power consumption of logic chips. The planar MOSFET has already evolved to a FinFET, a three dimensional device architecture which provides lower leakage current. New channel materials are now therefore considered to continue the transistor scaling and enable higher device densities with faster logic switching and lower power consumption. The III-V semiconductors which present electron velocities ten times higher than the silicon, are seriously considered as N-channel materials in a FinFET architecture for the sub-10nm technological node. To complete this integration, the development of plasma etching processes dedicated to the III-V fin patterning is necessary. The major challenge for nanometer-scale III-V finFET definition by plasma etching is the realization of vertical sidewalls with a high quality surface.

In this work, we address this challenge by undertaking a systematic investigation of dry etch processing for InGaAs fin formation, with the aim of obtaining high resolution fins with vertical sidewalls and clean etch surfaces. The InGaAs layers have been grown by MOCVD on 200mm Si wafer and photoresist lines with dimensions ranging from 20 to 100nm have been patterned by ebeam lithography. The plasma etching experiments are carried out on a 200mm etching platform from AMAT composed of two inductive coupled plasma reactors, whose one is equipped with a hot cathode. The performance of Cl_2 and CH_4 based plasma processes at 50°C and 200°C have been evaluated and compared in terms of anisotropy, surface roughness and plasma induced chemical damages. A particular attention is paid on the chemical and physical damages induced on the pattern sidewalls. The pattern profiles are characterized by electron microscopies. The sidewalls roughness is measured by AFM using a homemade setup where the sample is tilted to allow the tip to scan the sidewalls. The sidewalls chemical composition and stoichiometry after etching is analyzed by nanoauger spectroscopy. We also investigate restoring processes to mitigate the etch-induced sidewalls damages by combining oxidation and wet removal steps. Finally, we propose a new method to pattern the III-V fins without generating etching damages. It consists of a two-step process, starting with a surface

modification by a He or H_2 plasma implantation followed by a wet cleaning to remove the modified surface without damaging the non-modified one. This method appears promising to etch the III-V fin without damaging the fin sidewalls and will be benchmarked to conventional plasma technique.

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