

Plasma Science and Technology Room 104B - Session PS-MoA

Advanced BEOL/Interconnect Etching

Moderator: Hisataka Hayashi, Toshiba, Japan

1:40pm PS-MoA1 The Search for New Multi-Pattern Etch Colors: Usual (SiO_2 , SiN , SiC) and Unusual (hi-k, BN, BC:H) Suspects, *Michelle Paquette*, S. Dhungana, B.J. Nordell, A.N. Caruso, University of Missouri-Kansas City; W.A. Lanford, University at Albany; G. Chollon, C. Pallier, F. Teyssandier, Université de Bordeaux, France; K. Scharfenberger, D. Jacob, S.W. King, Intel Corporation

To continue the aggressive scaling of integrated circuit feature size demanded by current and future technology nodes, the microelectronics industry has turned to multiple patterning techniques to overcome lithography limitations. These techniques use a series of lithography and etch pattern transfer steps that require a variety of photoresist, hardmask, spacer, etch stop, and other specialized layers. These various pattern transfer materials can be categorized into 'colors,' where each color can be uniquely processed. As multiple patterning designs become increasingly complex, a number of different patterning materials with near-perfect etch selectivity will be needed, for which the current selection of materials will not suffice. Many previous etch studies have investigated the effects of plasma conditions on etch rates for common classes of metal and dielectric materials, but fewer have looked at the dependence of etch rates on material composition within a given class, and fewer still have analyzed the relative etch rates of multiple material classes and compositions under identical treatment conditions. We have surveyed etch rates for a wide range (>300) of samples using two common fluorinated etches traditionally used to pattern silicon-oxide-based (CHF_3) and silicon-nitride-based dielectrics (CF_4/O_2). These samples were drawn from material classes falling within the common Si-C-O-N-H composition space (e.g., SiO_xH , $\text{SiO}_x\text{C}_y\text{H}$, $\text{SiN}_x\text{C}_y\text{H}$), as well as classes not traditionally considered for patterning applications including hi-k dielectrics (e.g., Al_2O_3 , HfO_2) and boron-rich solids (e.g., BN:H, BP:H, BC:H). Surveying such a wide range of materials with varying densities and chemical stoichiometries has allowed us to look at both the effect of composition on etch rates as well as the relative etch rates between classes. From this information, we are able to propose materials that may serve as additional etch colors, drawn from within the classes studied, and by extrapolating the observed trends to different composition spaces.

2:00pm PS-MoA2 An Investigation into the Mechanism of High Selectivity SiO_x and SiN_x Dielectric Etching, *Robert Bruce*, H. Miyazoe, N.P. Marchack, IBM Research Division, T.J. Watson Research Center; J. Lee, J.C. Shearer, IBM Research, Albany, NY; J.M. Papalia, S.U. Engelmann, E.A. Joseph, IBM Research Division, T.J. Watson Research Center; J.C. Arnold, IBM Research, Albany, NY

As the semiconductor industry drives critical dimensions smaller for 7nm technology node and beyond, the challenges to dielectric etch for logic and memory chip manufacturing become ever greater. The established method of high performance dielectric etching is to employ a plasma process using a fluorocarbon (FC) gas that provides material-dependent selective deposition and sidewall passivation as the etch proceeds. Depending on the FC gas chemistry, SiO_x will etch selectively over SiN_x or vice versa. We investigate dielectric etch process parameters that influence dielectric material selectivity ($\text{SiO}_x/\text{SiN}_x$ or $\text{SiN}_x/\text{SiO}_x$) and pattern fidelity, including gas type and wafer temperature. We also study the possibility of improving selectivity by separating the FC deposition and etching steps (i.e. atomic layer etching).

2:20pm PS-MoA3 The Impact of Highly Selective Dielectric Etches on Etch Stop Layers, *Andre Labonte*, GLOBALFOUNDRIES; A. Carr, IBM; J.M. Dechene, GLOBALFOUNDRIES; J.C. Shearer, IBM; J.M. Lucas, B. Messer, A. Metz, Tokyo Electron America

As the semiconductor industry drives to sub 50nm gate and interconnect pitches, aspect ratios of contact and via structures are increasing. Subsequently, dielectric and etch stop layers are being thinned to mitigate the increase in aspect ratios. Likewise, the ongoing pursuit of scaling, without proportional changes in overlay, are driving the need for ever more selective Self-Aligned Contact (SAC) dry etch processes. As with any plasma, there is the potential to cause plasma damage to exposed surfaces and stop layers. The plasma damaged materials may in turn be susceptible to significant changes in their properties which may enhance or inhibit

future removal of the stop layer. Finally, due to the thinner stop layers being used, this change of material properties in a plasma damaged layer may not be limited to the surface of the layer, but may in fact convert the entire film.

In this paper, we discuss an example where a dielectric system, etched with a SAC process, exhibited an unexpected change in the material properties of the underlying etch stop layer. Process partitioning and materials analysis were used to confirm the unexpected result and develop a theory for observed changes.

2:40pm PS-MoA4 Plasma Etching of High Aspect Ratio Contacts in SiO_2 using $\text{Ar}/\text{C}_4\text{F}_8/\text{O}_2$ Mixtures: A Computational Investigation, *Shuo Huang*, C.M. Huard, University of Michigan; S. Shim, S. Lee, I.-C. Song, S. Lu, Samsung Electronics Co., Ltd.; M.J. Kushner, University of Michigan

As feature sizes continue to shrink and aspect ratios continue to increase in semiconductor processing, maintaining critical dimensions (CDs) of the features becomes more challenging. This is particularly the case for dielectric etch of high aspect ratio (AR) contacts (HARC), in which aspect ratios of 50-100 are desired. Our interests in this investigation are two challenges in the reactive ion etching of HARC in SiO_2 using $\text{Ar}/\text{C}_4\text{F}_8/\text{O}_2$ mixtures. The first is aspect ratio dependent etching (ARDE) where etch rates generally decrease as AR increases. The second is the origin of non-circular vias from nominally initially circular mask openings.

We report on results from a computational investigation of etching of HARCs in SiO_2 using $\text{Ar}/\text{C}_4\text{F}_8/\text{O}_2$ mixtures in a tri-frequency capacitively coupled plasma. Modeling of reactor scale and surface chemistry was performed using the Hybrid Plasma Equipment Model (HPEM). The feature scale modeling was performed using a 3-dimensional implementation of the Monte Carlo Feature Profile Model (MCFPM). The reactor utilizes 3 frequencies, two lower frequencies generally less than 10 MHz and 1 higher frequency of 50-100 MHz. For total powers approaching and exceeding 10 kW, radical fluxes to the wafer are dominated by CF_x , O and F due to there being significant dissociation of feedstock gas. Ion fluxes are dominated by Ar^+ and C_nF_m^+ .

The general trend of ARDE is observed - etch rates decrease with etch depth within a feature and features simultaneously etched show lower etch rates in smaller features. However, peaks in the instantaneous etch rate may occur when the profile becomes tapered, which funnels hot neutrals to the etch front. Factors contributing to ARDE such as molecular transport of neutral species, shading of ions with non-normal incidence and etch front geometry will be discussed. The origin of non-circular vias is likely due to small asymmetries and imperfections in the mask, which are reinforced during the etch process.

Work was supported by Samsung Electronics Ltd., Department of Energy Office of Fusion Energy Science and the National Science Foundation.

3:00pm PS-MoA5 BEOL & Interconnect Challenges in Memory Scaling, *Mark Kiehbauch*, Micron Technology **INVITED**

Interconnect challenges in memory are driven by scaling, novel architectures, and novel memories.

As NAND and DRAM scale, the pitch of the lower levels of metal routing shrink concurrently. With the delay in EUV lithography, 193 immersion together with complex pitch multiplication and multipatterning schemes have been implemented. These have etch challenges with regard to LWR, selectivity, and feature scale CDU.

The implementation of so-called More than Moore in memory is primarily TSV and 3D packaging to deliver multichip memory packages with extremely high bandwidth and also memory plus logic packages. Over the past several years, the integration of these technologies into high performance and cost effective packages has driven a continuous refinement of etch requirements.

Finally, new memory technologies have resulted in aggressive scaling of interconnects with unique profile and CDU requirements.

In each case, the process, hardware, and integration approaches to address these problems will be discussed.

4:00pm PS-MoA8 Control of Uniformity and Ion Energy Distributions in Tri-frequency Capacitively Coupled Plasmas Accounting for Finite Wavelength Effects, *Peng Tian*, S. Huang, University of Michigan; S. Shim, S. Lee, I.-C. Song, S. Lu, Samsung Electronics Co., Ltd.; M.J. Kushner, University of Michigan

To provide additional means of control of capacitively coupled plasmas (CCPs) for semiconductor processing, multi-frequency systems are being investigated. Current plasma tools now have up to 3 frequencies. The

source is typically a high frequency (50-150 MHz) intended to control ionization. The biases, typically low frequencies of a few to 10 MHz, are used to control ion energy distributions. At sufficiently high frequencies, the applied power takes on electromagnetic properties (as opposed to electrostatic) in which the electric field is wave-guided by the plasma sheath, causing constructive and destructive interference over the wafer. In extreme cases, a center-high electric field is produced along with a non-uniform center-high plasma density. The mixing of frequencies in tri-frequency systems (TF-CCPs) has the potential to mitigate finite wavelength effects while also providing opportunities to control IEDs.

In this work, TF-CCPs were investigated using a 2-dimensional hydrodynamic model with a full-wave FDTD (finite-difference-time-domain) solution of Maxwell's equations. Results will be discussed for plasma uniformity and IEDs for Ar and Ar/C₄F₈/O₂ gas mixtures at 10s of mTorr, with frequencies of a few MHz, 10 MHz and up to 150 MHz with collective powers of up to 10-15 kW. We found that at these elevated powers, the ability to separately control ion fluxes and IEDs is at best difficult. For these conditions, the system should be viewed as a collective set of 3-frequencies that have symbiotic contributions, as opposed to separate contributions that can be uniquely controlled.

Work was supported by Samsung Electronics Ltd., Department of Energy Office of Fusion Energy Science and the National Science Foundation.

4:20pm PS-MoA9 Metal Etch Mechanisms Using NH_x and CN-based Chemistry, Nathan Marchack, IBM Research Division, T.J. Watson Research Center; *M. Yamazaki, Q. Yang, N. Joy*, TEL Technology Center, America, LLC; *S.U. Engelmann, E.A. Joseph*, IBM Research Division, T.J. Watson Research Center; *A. Ranjan*, TEL Technology Center, America, LLC

While numerous processes for generating volatile metal etch products have been established in the field of plasma processing, there remain certain families of elements, e.g. ferromagnetic transition metals and their alloys, which have yet to display similar etch mechanisms. These and similar elements are finding increasing utility in novel memory technologies and thus their patterning at shrinking length scales poses an interesting problem for future technology nodes.

The existence of gas phase organo-metallic precursors such as M[(CO)]_x (where M = Ni, Fe, Co, etc.) has piqued curiosity in seeking pathways to generate such species using NH₃/CO chemistry in the literature[1], however experimental observation of such byproducts in the gas or plasma phase through techniques such as mass spectrometry has not been reported[2]. Older literature may suggest alternative mechanisms involving the reaction of such metals in the gas phase with linear nitriles[3] and amines[4]. We explore potential reactions of such organic species generated in a variety of high density plasma sources, with a focus on defining how parameters such as source power, type, and gas ratio affect the discharge properties.

The results of this study will then be applied to patterned film stacks of commonly reported metal elements (e.g. Ni, Fe, Co) demonstrating a potential means for etching these materials at tighter pitches (<200nm) for line/space and pillar geometry with reduced sidewall residue and minimal hard mask loss.

References:

- [1]: Kubota et al., Journal of Magnetism and Magnetic Materials, 272-276, 2004.
- [2]: Jeon et al., Journal of Vacuum Science and Technology A, 33, 061304, 2015.
- [3]: Lebrilla et al., Journal of American Chemical Society, 109, 5639-5644, 1987.
- [4]: Radecki and Allison, Journal of American Chemical Society, 106, 946-952, 1984.

4:40pm PS-MoA10 The Impact of Gate Overlap on Self-Aligned Contact (SAC) Etching, Jeffrey Shearer, IBM Research Division, Albany; *A.P. Labonte*, GLOBALFOUNDRIES; *J.M. Lucas, A. Metz*, Tokyo Electron - TTCA; *J.C. Arnold*, IBM Research Division, Albany

In order to maintain aggressive scaling trends, gate and contact pitches have been reduced to a level requiring robust contact-to-gate self-alignment in order to mitigate gate-to-contact short concerns. Developing novel reactive ion etch (RIE) chemistries to achieve the necessary etch selectivity to the gate cap is one of the more critical challenges in integrated circuit (IC) process development and manufacturing. Further complicating the process space is that selectivity is impacted by the contact-to-gate overlap. This overlap can be intentionally modulated by pitch demands, mask design, and contact critical dimension (CD) or

unintentionally modulated by contact-to-gate overlay shifts. Data will show a substantial difference in selectivity between one-sided (borderless) and two-sided ("true SAC") contact-to-gate overlaps. As both situations could exist on-wafer, it is increasingly difficult to develop robust processes that can accommodate a variety of different contact designs at the same time. The data will show how process optimization can minimize some of the challenges in developing a robust process space and will explore the parameter space that can maximize the SAC selectivity process window across multiple overlap regimes. Lastly, it will be shown how overetch impacts the selectivity of the gate cap in terms of the contact-to-gate overlap. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

5:00pm PS-MoA11 Dynamic Plasma Etching of EUV Photoresist for Contact Profile Control and PR Selectivity Improvement, Hongyun Cottle, I. Saraf, A. Metz, P. Biolsi, TEL Technology Center, America, LLC

Continued pitch scaling of semiconductor devices to 7nm node and beyond dimensions utilizing conventional 193i based multiple patterning techniques is rapidly driving up cost, complexity, and variability control. EUV patterning can be used to mitigate or delay the challenges of pitch scaling through multiple patterning, but introduces new challenges of its own. EUV lithography introduces new types of resists that are thinner and less etch resistant compared to conventional 193nm resists. Interactions of polymers with plasma etch environments can lead to large changes of the polymer material properties and the three-dimensional nanostructures they pattern. Mask deformation during such etch process can lead to changes in nanoscale topography of device features, often with undesirable consequences, such as increased LER and LWR, tip-to-tip degradation, and line wiggling. Plasma etch faces a significant challenge to optimize its process window to enable high yields with EUV patterning.

This paper presents an unique etch process employing a dynamic etch during softmask open to improve EUV photoresist etch selectivity by greater than two fold while maintaining critical feature dimensions, such as elliptical contact minor vs major axis CD ratio. By carefully controlling the polymer deposition vs. polymer assisted etching temporal cycle, a very thin layer of conformal polymer can be used to precisely etch and transfer the desired pattern. By utilizing a direct current superposition (DCS) technology, EUV photoresist can be treated to improve not only its etch resistant, but also LER and LWR. After the in-situ photoresist treatment, the dynamic etch process initiates and defines the pattern transfer into softmask, followed by etch steps to anisotropically complete the pattern transfer. Reported is the structural characterization pre and post-etch detailing LER and LWR improvement, and shrink ratio control. In addition, a mechanistic model will be proposed based on optical emission spectroscopy (OES) and thin film compositional analysis.

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