Manufacturing Science and Technology
Room 103A - Session MS+AS-TuM

Characterization and Processing for IC Manufacturing

Moderator: Alain C. Diebold, SUNY College of Nanoscale Science and Engineering

8:00am **MS+AS-TuM1 Thermal Decomposition Properties of Bis(cyclopentadienyl)magnesium for Various Gas Supply System Materials***, **Hidekazu Ishii**,* Tohoku University, Japan*; S. Yamashita, M. Nagase, A. Hidaka, K. Ikeda,* Fujikin Incorporated, Japan*; Y. Shiba, Y. Shirai, S. Sugawa,* Tohoku University, Japan

High purity Bis(cyclopentadienyl)magnesium(Cp_2Mg) is used as chemical vapor deposition material of semiconductor devises and dopant for obtaining p-type conduction in GaN based material devices. However, precise control of supply concentration of Cp_2Mg is very difficult because its vapor pressure is very low. Generally, Cp_2Mg is supplied from a precursor container to the film formation chamber by bubbling with the carrier gas. In this method, the tubing for the gas supply must be heated to avoid deposition of Cp_2Mg on the inner surface of tube, which leads to a concern of decomposition of Cp_2Mg. Thus, understanding of thermal decomposition properties of Cp_2Mg for various materials for gas supply tube is important. In this report, we report evaluation results of thermal decomposition properties of Cp_2Mg for various materials such as SUS316L stainless steel and Cr_2O_3, Al_2O_3-passivated stainless steel that are used for gas tubing, as well as Ni-Co alloy and Hastelloy C-22 that are used for a valve diaphragm.

8:40am **MS+AS-TuM3 High Volume Materials Characterization in the CMOS Industry***, **Paul van der Heide**,* GLOBALFOUNDRIES **INVITED**

In no time in the past has Materials Characterization been as pivotal to CMOS device R&D as it is today. This stems primarily from the fact that since the era of *Denard scaling* (shrinkage alone), new materials/ structures have had to be introduced in order for logic devices to continue to adhere to the dimension shrinkage implied by *Moore's law* (examples lie in the introduction of strain engineering (introduced in 90nm devices rolled out in 2003), HKMG structures (introduced in 45nm devices rolled out in 2007), and 3D structures (introduced in 22nm devices rolled out in 2011)). This timeline also begs the question: A*re we not at the precipice of the next innovation?* What is certain is that the CMOS industry will experience significant and in some cases unforeseen changes over the next 2 decades.

Materials characterization is not only needed to support R&D efforts, but is also required to provide insight into manufacturing issues, along with the qualification of a) new fabrication processes, b) new process equipment, and c) process equipment coming off preventative maintenance cycles. Paramount in these areas is analytical precision, repeatability, data quality and speed (turn around time). This stems from the other aspect of *Moore's law*; that being that the cost associated with the development/implementation of a new device node must remain financially attractive. Topics covered in this presentation include: the support requirements of a high volume CMOS manufacturing site, merits of academia versus industrial labs, financial justifications of onsite lab/s, along with some recent analytical examples/capabilities.

9:20am **MS+AS-TuM5 Dynamics in SIMS Characterization for Advanced Nano-Technology: Challenges and Solutions for Novel Materials and 3-D Devices***, **Marinus Hopstaken**,* IBM T.J. Watson Research Center **INVITED**

Over the last few decades, SIMS depth profiling techniques and instrumentation has tremendously evolved to keep up with developments in advanced CMOS technology. I will discuss the main technology drivers, their implications for SIMS characterization, and review some of the analytical challenges and solutions:

- Continued dimensional scaling (*i.e.* lower film thicknesses, ultra-shallow junctions USJ) demands for progressive improvement of depth resolution. This has been enabled by continuous instrumental developments to provide high-density, stable, and low-impact energy primary ions beams to enable sub-nm depth resolution (*i.e.* 'Atomic layer' SIMS). I will give various applications of high resolution SIMS analysis of thin-film stacks / USJ, routinely employing sub-500 eV ion beams

- Advanced IC development in a manufacturing context demands at-line SIMS metrology with high throughput and reproducibility, often requiring small area analysis on patterned wafers. Key enablers for advances in SIMS metrology are availability of high-density primary ion beams, high level of automation to allow for unattended operation, and instrumental stability / drift correction. I will discuss implications for high-throughput SIMS full wafer mapping and considerations for patterned device wafer

- Paradigm shift towards 3D device architectures (*i.e.* FinFET) poses one of the greatest challenges, and appears fundamentally incompatible with low-energy (*i.e.* 'broad-beam') SIMS. This can be partially circumvented by averaging over a large regular arrays of FinFET structures, in combination with backfill and planarization to delineate the Fin sidewall ('SIMS through Fin technique;), which we have successfully employed at realistic Fin dimensions and pitch, relevant for 14 nm node and beyond

- Integration of novel and dissimilar material stacks demands novel SIMS calibration methods and/or quantification protocols. Potential solutions to deal with the higher complexity are cross-calibration with absolute external techniques (ion scattering techniques, 3D-APT, advanced TEM-EDX / EELS, etc…) and multi-standard approaches for explicit correction of SIMS yield variations with matrix composition. I will give selected examples for quantification of in-situ doping in $SiGe_x$ for wide variation in Ge% and different doping species in various III-V compounds

11:20am **MS+AS-TuM11 Characterization of Electrical Properties of Si and GaN Devices using Scanning Microwave Impedance Microscopy (sMIM) and Nano-scale Capacitance-voltage Curves***, **Stuart Friedman**, F. Stanke, Y. Yang, O. Amster,* PrimeNano, Inc

The use of Atomic Force Microscopy (AFM) electrical measurement modes is a critical tool for the study of semiconductor devices and process development. A relatively new electrical mode, scanning microwave impedance microscopy (sMIM), measures a material's change in permittivity and conductivity at the scale of an AFM probe tip [1]. sMIM provides the real and imaginary impedance (Re(Z) and Im(Z)) of the probe sample interface. By measuring the reflected microwave signal as a sample of interest is imaged with an AFM we can in parallel capture the variations in permittivity and conductivity and, for doped semiconductors, variations in the depletion layer geometry. An existing technique for characterizing doped semicondutors, scanning capacitance microscopy, modulates the tip-sample bias and detects the tip-sample capacitance with a lock-in amplifier. A previous study compares sMIM to SCM and highlights the additional capabilities of sMIM [2].

In this talk we focus on the detailed mechanisms and capabilities of the nano-scale C-V curves that can be obtained using sMIM to measure the tip-sample capacitance as a tip-sample bias is swept. Analogous to traditional macro-scale capacitance-voltage experiments, the nano-scale C-V curves probe properties such as doping concentration through their influence on the voltage dependent geometry of the depletion layer. In particular, in this talk we will address the ability to extract semiconductor properties, such as doping concentration, from the C-V curves. This study includes analytical and finite element modeling of tip-bias dependent depletion layer geometry and impedance. These are compared to experimental results on reference samples for both doped Si and GaN doped staircases to validate the systematic response of the sMIM-C channel to the doping concentration.

[1] S. Friedman, O. Amster, Y. Yang, "Recent advances in scanning Microwave Impedance Microscopy (sMIM) for nano-scale measurements and industrial applications." Proceedings of the SPIE, Volume 9173, id. 917308 8 pp. (2014)

[2] B. Drevniok, St.J. Dixon-Warren, O. Amster, S.L. Friedman, and Y. Yang, "Extending Electrical Scanning Probe Microscopy Measurements of Semiconductor Devices Using Microwave Impedance Microscopy", Proceedings of the 41st International Symposium on Testing and Failure Analysis (2015), pp. 77.

11:40am **MS+AS-TuM12 Results of the 2016 Triennial Review of the National Nanotechnology Initiative***, **James Murday**,* University of Southern California*; B.R. Rogers,* Vanderbilt University*; E.B. Svedberg,* The National Academies **INVITED**

The National Nanotechnology Initiative is a multi-agency effort to advance nanoscale science, engineering, and technology and to capture the associated economic and societal benefits. The NNI comprises the collective activities and programs among the more than two dozen participating federal agencies with diverse missions and presently a total annual investment of approximately $1.5 billion. Every three years the National Academies selects a committee of experts to review the NNI in accordance with the provisions of the 21st Century Nanotechnology Research and Development Act. A report on the most recent review has just been released. This report has paid particular attention to examining and commenting on the physical and human infrastructure needs for successful realization in the United States of the benefits of nanotechnology development and also the mechanisms used by the NNI to advance focused areas of nanotechnology towards advanced development and commercialization. We will report the findings and recommendations of this review.

Author Index

Bold page numbers indicate presenter