Electronic Materials and Photonics
Room 102A - Session EM+MN-TuM

New Materials and Devices for TFETs, Spintronics, and Extended CMOS

Moderator: Wilman Tsai, TSMC

8:40am **EM+MN-TuM3 Tunneling FET Technology using Ge and III-V Semiconductors**, ***Shinichi Takagi***, *M. Takenaka,* The University of Tokyo, JST-CREST, Japan **INVITED**

Since TFETs based on band-to-band tunneling are expected as ultra-low power devices applicable to LSI for IoT , development of the optimum materials, structures and fabrication process have been strongly pursued for realizing both low sub-threshold swing (SS) of sub-60 mV/dec. and high drain Ion/Ioff ratio at the same time. For this purpose, the reduction in the effective band gap is important for enhancing tunneling current. Thus, we are currently focusing planar-type TFETs using Ge/III-V and their hetero-structures.

In this talk, we address two types of planar TFETs utilizing the Ge/strained Si (sSi) hetero-structure and the InGaAs channels. One of the key issues for TFETs is the formation of the steep and high quality source junctions, which provide both high tunneling current and low off current. For InGaAs TFETs, we have introduced solid-phase Zn diffusion through utilizing the inherent diffusion property of Zn in InGaAs creating defect-less extremely-steep profiles. The steepness of the Zn profiles less than 3.5 nm/dec. was obtained, thanks to the diffusion constant of Zn in InGaAs proportional to the square of the Zn concentration, leading to the automatic realization of the steep impurity profile. The small SS of 64 mV/dec and large Ion/Ioff ratio over1E6 have been realized in the planar-type InGaAs TFETs at room temperature.

For tensile strain Si channel TFETs with Ge sources, in-situ doping p+ Ge/sSi source junctions are employed for realizing steep and defect-less tunneling junction formation. Here, the higher Ev edge of the Ge-source and the lower Ec edge of tensile-strained Si result in reduction in the effective band gap, leading to the increase the tunneling probability with maintaining the relatively large Eg of sSi in the drain regions, which can suppress the ambipolar leakage current. The fabricated Ge/sSOI (1.1 %) TFETs show high Ion/Ioff ratio over 1E7 and steep minimum SS of 28 mV/dec.

In conclusion, the enhancement of tunneling probability by utilizing III-V/Ge materials is quite effective in improving the performance of TFETs. Superior source junction formation and MOS interface control technologies are key factors to realize TFETs using III-V/Ge.

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9:20am **EM+MN-TuM5 Thin Film Materials in Novel Spintronic Devices**, ***Gang Xiao***, Brown University **INVITED**

Tomorrow's spintronic MRAM (Magnetic Random Access Memory) and logic processors could exploit the physics of the giant spin Hall effect (GSHE) for switching bits, but the materials engineering is challenging. Solids with large atomic numbers and resistivities exhibit very large Spin Hall Angle (SHA), a key and characterizing parameter of GSHE. The origin of GSHE is the enhanced spin-orbit coupling (SOC), based on which the search on solids with even larger SHA continues. Some of these solids are difficult to fabricate due to their metastable structures. We have realized robust perpendicular magnetic anisotropy (PMA) in a layered structure combining the elusive, metastable β phase of tungsten and a ferromagnetic thin film. The large spin-orbit coupling in β-W yields, after suitable annealing, a very low critical current density for magnetization switching. Our structures furthermore are easily fabricated, making them even more technologically promising and compatible to modern semiconductor fabrication process.

11:00am **EM+MN-TuM10 Tunneling in Low-Dimensional Materials**, ***Joerg Appenzeller***, Purdue University **INVITED**

Over the last years, two-dimensional (2D) materials are attracting an increasing amount of interest for various electronic applications owing in particular to the ideal electrostatics conditions that can be enabled in a three-terminal field-effect transistor (FET) geometry. Transition metal dichalcogenides (TMDs) as MoS_2, WSe_2, or WS_2, to just name a few, or black phosphorus (BP) offer sizable bandgaps at mobilities that cannot be achieved in three-dimensional, bulk type materials that are scaled down to similar dimensions. The key is the absence of dangling bonds at the 2D semiconductor to substrate or gate dielectric interface that allows for highly conductive channels with sub-nm body thicknesses. In my presentation I will discuss the benefits of an ultra-thin body structure for scaled device applications with a particular emphasis on tunneling field-effect transistors (TFETs). I will also elucidate the critical impact of Schottky barrier (SB) contacts in the context of TMD and BP devices and will present an analytical approach that allows extracting materials and device information as the SB height and bandgap of single- and multi-layer FET structures. Moreover, I will present an analysis on the impact of strain in TMD FETs and discuss the potential relevance of strain for TMD TFETs to achieve ideal performance specs.

11:40am **EM+MN-TuM12 Controlled Phase Transition for Ultra Low Power Transistors**, ***Sayeef Salahuddin***, University of California, Berkeley **INVITED**

Phase transition materials have long been investigated for fundamental physics and also for potential application in electronics. In this presentation, I shall discuss how a controlled phase transition can lead to fundamentally new switching devices that has significantly less energy dissipation compared to the state of the art. In particular, I shall talk about the state of negative capacitance that can be achieved in certain material systems with stored energy of phase transition. Our recent experiments with ferroelectric materials have shown that such a state of negative capacitance can actually be achieved. I shall also describe our very recent results where such negative capacitance, when combined with conventional transistors, have demonstrated a reduction in supply voltage at a given ON current.

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