Tuesday Morning, October 20, 2015

Plasma Science and Technology
Room: 210B - Session PS-TuM

Advanced BEOL/Interconnect Etching
Moderator: Tetsuya Tatsumi, Sony Corporation, Japan

8:00am **PS-TuM1 Interconnect Patterning in the EUV Era**, ***John Arnold***, IBM Research Division, Albany, NY **INVITED**

The semiconductor industry is currently passing through a pivotal moment as EUV lithography transitions from patterning research to industrial-scale integrated technology development. This change will have ramifications far beyond the lithography itself, including impacts on adjacent unit processes, process complexity, development and manufacturing cycle times, product cost, and product yield, quality, and reliability. The most direct and immediate changes will be in plasma etch, where the combination of new materials and new dimensions will drive significant new challenges – and opportunities. The timing of EUV's readiness for practical utilization is such that most of the initial applications will be at the wiring levels, both BEOL and MOL, and this presentation will focus on those. We will begin with an examination of EUV's placement in the overall technology roadmap and a review of the important differences between EUV and conventional lithography. The bulk of the presentation will be dedicated to applications for contact, local interconnect, and BEOL, with particular emphasis on lithography and especially etch process behavior and performance. A discussion of the operational ramifications of incorporating EUV into a mainstream technology development program will be followed by a brief consideration of the anticipated benefits for the final manufactured products. We will conclude with a critical comparison of EUV to 193nm-based multiple patterning approaches for the 7nm node.

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development facilities.

8:40am **PS-TuM3 Challenges for the sub-32nm Pitch Self-aligned Quadruple Patterning (SAQP) at Back End of Line (BEOL)**, ***Nihar Mohanty***, *R. Farrell, A. Raley, E. Franke, J. Smith, S. Song, A. Ko, A. Ranjan, A. deVilliers, P. Biolsi*, TEL Technology Center, America, LLC, *W. Wang, G. Beique, C. Labelle, L. Sun, R. Kim*, Globalfoundries, Ny, Usa

Critical back end of line (BEOL) M_x patterning at 7nm technology node requires sub-36nm pitches necessitating the use of either extreme ultraviolet (EUV) lithography or 193nm-immersion-lithography based self-aligned quadruple patterning (SAQP). With enormous challenges being faced in getting EUV lithography ready for production, SAQP is expected to be the front up approach for M_x grid patterning for most of industry. In contrast to the front end of line (FEOL) fin patterning, which has successfully deployed SAQP approach since 10nm node technology, BEOL M_x SAQP is challenging owing to the required usage of significantly lower temperature budgets for film stack deposition. This has an adverse impact on the material properties of the as-deposited films leading to emergence of several challenges for etch including selectivity, uniformity and roughness.

In this presentation we will highlight those unique etch challenges associated with our BEOL Mx SAQP patterning strategy and summarize our efforts in optimizing the etch chemistries, process steps and plasma etch parameters for meeting the 7nm technology node targets. With the mandrel definition parameters being the most significant input function for final pattern performance, we will detail our efforts in improving the CD uniformity (CDU), profile and line edge roughness (LER) / line width roughness (LWR) for both the mandrel definition etches. All of the etch development for this work has been conducted in our dual frequency capacitively coupled plasma (CCP) chamber with optimized gap for good baseline uniformity and independent ion flux & energy control.

9:00am **PS-TuM4 Novel Patterning Process for the 7xnm and Beyond**, ***Toru Hisamatsu***, Tokyo Electron Miyagi Limited, Japan, *T. Oishi, S. Ogawa,* Tokyo Electron Miyagi Limited*, Y. Kihara, M. Honda*, Tokyo Electron Miyagi Limited, Japan

Multiple exposures with double (quadruple) patterning has been adopted due to recent advancements in miniaturization with mask patterning techniques, and as the technology continues to develop, EUV exposure will be used in the near future. Extending the current techniques into the next generation is approaching the limit to satisfy required fabrication specifications, as it is required to have fabrication control of less-than- a-nm-order.

In the patterning process, multilayer patterning with high accuracy to form a fine patterning is becoming critical, especially in regards to line-roughness (LER/LWR) reduction, pattern-size dependency reduction of ARDE origin, and selectivity enhancement of thin EUV-resist. Furthermore, patterning with universal CD shrinkage independent of the pattern types (hole, oval, L/S) is also being required.

To this date, challenges of precise CD controllability have been solved by combining DC-superimposed plasma which reduces line-roughness by its accelerated electron-beam to cure resist surface, followed by the Si coating effect and optimization of etch condition to form a protection layer on the surface[1,2]. However, it is evident that those current techniques will soon face the limit as the resist thickness is reduced with the employment of EUV exposure; therefore the breakthrough with the new approach is essential.

As a result of various feasibility studies put into effect for a problem solution of fine pattern formation, "fusion of ALD technology and etching" was confirmed to be very beneficial for its capability of atomic-level formation of surface protection film during the etch process. This technology enabled line-roughness reduction with pattern-size dependent CD shrink control, since the ALD step is used according to the optimum timing during the etch process, which forms proportional deposition on any type of patterns. This paper discusses the optimization of ALD step timing, its layer thickness and composition of corresponding etch flow, and introduces a possible solution to various patterning process issues without trade-offs. This technique enables atomic-level control during the etch process and thus, is promising for further miniaturization of the patterning process.

Reference

[1] M. Honda et al., AVS 60th Int. Symp. & Exhibit. (2013)

[2] M. Honda et al., Proc. of SPIE 8328-09 (2012)

9:20am **PS-TuM5 Advanced Interconnect Process Techniques with EUV Photolithographic Masks and Sub-50nm Pitch Structures**, ***Jessica Dechene***, *J.C. Shearer,* IBM Research Division*, A.P. Labonte,* GLOBALFOUNDRIES*, J. Lucas, H. Matsumoto, B. Messer, A. Metz,* TEL Technology Center, America, LLC, *C. Labelle,* GLOBALFOUNDRIES*, J.C. Arnold*, IBM Research Division

As the semiconductor industry moves into the sub-10nm technology nodes, feature pitches below 50nm become ubiquitous. To avoid the complications of SADP processing, EUV photolithography is being explored as a means to continue direct patterning. This brings forth etch processing challenges in three ways: First, EUV resists are thinner, softer and suffer from greater LER than 193nm optical resists. Second, the small dimensions and tight pitches are causing old problems, once thought of as solved, to reappear. Pattern collapse, aspect ratio dependent etching, ion deflection induced profile bowing, and feature induced CD variation are a few examples. Third, new integrations seeking the use of self-alignment, including self-aligned etch are becoming more prevalent. These self-aligned methods at such small dimensions require innovated etch techniques in order to be enabled.

In this paper, we will discuss the theory behind the various process solutions used to solve these etch challenges. Bias pulsing was used to address aspect ratio dependent etching concerns, and gas pulsing was used to improve material and corner selectivity in a self align etch process. Dielectric etch process solution on a dual-frequency capacitively coupled plasma (CCP) system were applied to the EUV lithographic masks. Superimposing a negative DC voltage to control the emission of ballistic electrons along with chemistry balance was used to minimize feature-dependent etch CD bias. These innovative process options allowed for the development of dielectric RIE processes that hit target specifications in the demanding pitch and CD sizes generated by the EUV lithography.

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities.

9:40am **PS-TuM6 Advanced Plasma Etch Techniques for Sub-50nm Pitch Contact & Interconnect Etches**, ***Andre Labonte***, Globalfoundries, NY, USA*, R. Chao, J.M. Dechene,* IBM Albany Nanotech Center, *B. Nagabhirava, P. Wang, P. Friddle,* Lam Research*, N. Rassoul,* ST Microelectronics, *C. Labelle,* Globalfoundries, NY, USA*, J.C. Arnold,* IBM Albany Nanotech Center, *M. Goss*, Lam Research

As the semiconductor industry drives into sub-50nm pitches, EUV patterning as well as SADP and SAQP techniques are being explored as means to achieve the desired CDs and pitches needed. EUV patterning is attractive for enabling direct patterning and in principle, is significantly less complicated than SADP, let alone SAQP. However, EUV patterning comes with its own set of challenges, such as softer and thinner resists relative to optical 193nm resists. Also, to date, EUV resists have exhibited more

LER/LWR than optical 193nm resists. Finally, the smaller features and pitches are resulting in the reoccurrence of old scaling issues such as RIE lag and pattern collapse. Many of these challenges are being met with innovative plasma etch techniques.

In this paper we discuss the theory behind many of the techniques used to solve the afore mentioned challenges associated with EUV and sub-50nm pitch patterning. In particular, RF pulsing and Bias pulsing are used to increase EUV resist selectivity, reduce LER/LWR, avoid pattern collapse and improve RIE lag in the dielectric etch. In addition we will also discuss the theory and application of AMMP (Advanced mixed mode pulsing) to improve the corner selectivity of low-k spacer in MOL to allow for the generation of self-aligned contacts. Finally, AMMP techniques were used to mitigate feature to feature CD variation incoming from litho.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

11:20am **PS-TuM11 Characterization of Patterned Porous Low-*k* Dielectrics after Plasma Patterning and Subsequent Wet Processing/Cleaning**, ***QuocToan Le**, E. Kesters, S. Decoster, B.T. Chan, F. Holsteyns,* IMEC, Belgium*, S. De Gendt*, IMEC, KU Leuven Belgium

Porous dielectrics have been commonly used in micro- and nanotechnologies since the past decade. Their chemical composition and porous properties make them more susceptible to physical and chemical damage. In particular, pattern etching and subsequent processes for removal of resist layers and/or post-etch residues are critical steps that potentially modify the dielectric properties [1].

This study first focuses on the modification of the porous dielectric material (pore structure, surface sealing, wettability) using a patterned line/trench test structure of 45 nm ½ pitch (Fig. 1). Several methods were applied for characterization of the patterned structure used in this study, including ellipsometric porosimetry (EP), X-ray photoelectron spectroscopy (XPS), and Fourier transform Infrared spectroscopy (FTIR). Fig. 2 shows the variation of the polarization state, expressed here by Delta angle, as a function of the relative pressure of toluene (used as a probe for porosity change). For the 45 nm patterned structure, the rapid change in Delta angle reflects the adsorption of toluene into the porous network. This clearly indicates that the patterned low-k surface remained unsealed after the C_4F_8/CF_4-based etch plasma process. In contrast, the surface of the blanket low-k film was almost sealed, evidenced by a very slow and irreversible toluene adsorption. Note that the sealing layer is only concerned the surface. The approach and characterization methods utilized for determination of the sealing thickness and the internal hydrophobic/hydrophilic properties [2] of the patterned porous low-k structures will be discussed.

Another aspect of this study concerns the surface composition of the patterned feature, type of the residues generated during the plasma etch, and the effect of a subsequent wet clean step. The latter is usually required before the deposition of the barrier layer. Substantial amount of fluorinated etch residues were detected on both the TiN surface and the dielectric sidewall and bottom. As shown in Fig. 3, the XPS F 1s core-level spectrum for the surface after the OSG etch consisted of two main components: the peak centered at ~684.6 eV corresponds to F-Ti bonds and the peak at 688.4 eV can be assigned to C-F bonds. The efficiency of the removal/dissolution of CFx and TiFx by the wet chemistries can be clearly demonstrated using this 45 nm test structure. For instance, dilute HF and TMAH:H_2O_2 mixture are efficient for TiFx removal but only show very limited dissolution of CFx polymer. In the presentation, the change in the low-k dielectric and TiN properties due to the plasma etch and subsequent wet cleans will also be presented and discussed.

11:40am **PS-TuM12 Cryogenic Etching of Porous Organosilicate Low-k Materials: Reduction of Plasma Induced Damage**, ***Floriane Leroy**, T. Tillocher,* GREMI CNRS/Université d'Orléans, France*, L. Zhang,* IMEC, KU Leuven, Belgium*, P. Lefaucheux,* GREMI CNRS/Université d'Orléans, France*, K. Yatsuda,* TEL, Japan*, K. Maekawa,* TEL Technology Center, America, LLC*, J.-F. de Marneffe, M. Baklanov,* IMEC, Belgium*, R. Dussart*, GREMI CNRS/Université d'Orléans, France

Porous Organosilicate (OSG) low-k materials were introduced as inter-metal dielectrics, in order to reduce RC signal delay and energy dissipation. Low-k value is achieved by enlarged open porosity and pore size, but integration of porous low-k is impeded by plasma induced plasma (PID). Several low-damage processes have been reported in the literature. Recently, cryogenic etch, using SF_6-based plasma, was studied as an alternative approach [1]. It was observed that the PID is reduced by decreasing the wafer temperature to cryogenic region (-120°C). At such a low temperature, a passivation layer forms on the pore sidewalls in the low-k bulk, and minimize reaction with damaging radicals.

In this work, we investigate the mechanisms behind this cryogenic low damage process on blanket sample glued on a SiO_2 carrier wafer. The etch rate and the refractive index were measured by in-situ ellipsometry and ex-situ FTIR was used to evaluate methyl group depletion. Species desorbed during the warm-up of the cooled OSG films were detected by a mass spectrometer mounted on the diffusion chamber. In the case of a pure SF_6 plasma, the main desorbed species are C_xF_y, SF_x, SO_xF_y and SiF_x. SOF_2^+ increases first from -120°C to -80°C and decreases from -80°C to 20°C, which shows that a strong desorption of SOF_4 occurs in this range of temperature and play a major role in SF_6 silicon etching [2]. SiF_3^+ and $C_2F_4^+$ mainly desorb at -60°C. It is known that SiF_4 is involved in passivation mechanisms for cryogenic etching, but this result suggests that fluorocarbon species also play a significant role. This is why it was proposed to add C_4F_8 to further protect the low-k material. This new SF_6/C_4F_8 chemistry was studied for various temperatures (from -120°C to +20°C). PID were minimized at -120°C and lower than with pure SF_6. In addition, the increase of the refractive index during the etching process reveals that C_4F_8 condenses into the pores, which is believed to enhance the protection of the material. The desorption of the C_xF_y, SF_x, and SiF_x species is still observed by mass spectrometry. It appears that SiF_3^+ and $C_2F_4^+$ peaks intensity exhibit two local maxima: -120°C, due to desorption of condensed C_4F_8, and -60°C, due to the desorption of the passivation layer. In addition, in-situ XPS experiments was carried out to determine the fluorine based stoichiometry of the passivation layer [3]. Finally, profiles etched with SF_6/C_4F_8 chemistry at -120°C will be presented.

[1] L. Zhang *et al.,* ECS J. Solid State Sci. Technol. 2(6), N131-N139 (2013)

[2] X. Melhaoui *et al.*, J. Appl. Phys 98, 104901 (2005)

[3] J. Pereira *et al.,* Appl. Phys. Lett. 94, 071501 (2009)

12:00pm **PS-TuM13 Remote Shielded Microwave Mini Plasma Source for Sample Cleaning**, ***Herman Bekman**, R.J. Bolt, F.A. Nennie, P.M. Muilwijk, F.T. Molkenboer, N.B. Koster, O. Kievit*, TNO Technical Sciences, Netherlands

In EUV contamination control, but also more generally, there is a desire for a cleaning technique that can remove hydrocarbon contaminants without inflicting damage to the underlying substrate, e.g. in electron microscopy. Plasma cleaning based on shielded microwave using hydrogen is such a cleaning technique. Generally microwave plasma cleaners are quite big, but at TNO we are pursuing miniaturized plasma cleaners to enable local in-situ cleaning.

In an earlier attempt a mini plasma cleaner has been developed based on a resonant cavity partially filled with a high dielectric material. The source could be operated inside a vacuum system. Due to unexpected thermal issues the source operated only a limited number of times. Furthermore we experienced that it was difficult to judge from the outside why the plasma source was not igniting anymore. A desire for detailed diagnostics during plasma ignition attempts was evident.

A second generation mini microwave plasma cleaner was subsequently designed, built, and tested. The aim was to realize a mini plasma cleaner that should fit on small load locks. Thus substrate could be cleaned prior or after an inspection/processing step. A microwave test setup was designed that allowed simultaneous supply of high power microwave signal at a fixed microwave frequency, for ignition of the plasma, and supply of a low power swept microwave frequency signal for resonator characterization.

This presentation will focus on realization and characterization of the mini plasma source. Cleaning rate as well as detailed microwave characterization measurements have been performed. The microwave measurements demonstrated in real time the effect of plasma ignition on resonance behavior of the cavity.

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