Plasma Science and Technology
Room: 210B - Session PS-MoM

Advanced FEOL/Gate Etching

Moderator: Chanro Park, GLOBALFOUNDRIES

8:20am **PS-MoM1 FEOL Patterning Challenges for Sub 14nm FDSOI Technology**, ***Sébastien Barnola***, *N. Posseme, P. Pimenta-Barros, C. Vizioz*, CEA, LETI, MINATEC Campus, France, *C. Arvet*, ST Microelectronics, France, *O. Pollet, A. Sarrazin*, CEA, LETI, MINATEC Campus, France, *M. Garcia-Barros*, ST Microelectronics, France, *L. Desvoivres*, CEA, LETI, MINATEC Campus, France **INVITED**

Fully-depleted SOI devices (FDSOI) are proven to provide excellent control of gate electrostatics. This makes them a real solution to meet performance requirements down to 10nm technology node, however new architectures such as stacked silicon nanowires will be required to maintain low leakage current when further downscaling gate length. Additionally new materials are required to build transistor channel complying with ON-state current expectations, such as new channel materials such as germanium or compound semiconductors or low k materials at the spacer level.

These changes in transistor integration raise quite a number of new challenges for etching and stripping in that they introduce new materials with uncommon properties compared to usual silicon-based devices.

Another challenging aspect of device downscaling is the enhanced demand for high-selectivity etch. In spacer definition for instance, maximum allowable silicon recess in source / drain regions is less than 0.5nm for the 14nm node. To this end new techniques are being developed that involve a prior modification of the etched layer down to a controlled depth, followed by the removal of the modified layer selectively to the non-modified material.

On the technology side, immersion 193nm lithography has reached its limits in resolution and the most critical levels require costly dual or quad-patterning technique to achieve stringent CD specifications in current 14nm and beyond. Solutions to further expand 193nm lithography capabilities at lower costs are showing promising results, such as sidewall image transfer (SIT) or directed self-assembly (DSA). Nevertheless these newly developed techniques involve process adaptations on the plasma etching side since they induce changes in the masking materials.

9:00am **PS-MoM3 Material and Etch Interaction Comparisons for SIT Patterning**, ***John Sporre***, IBM Corporation, *A. Raley*, TEL Technology Center, America, LLC, *D. Moreau*, STMicroelectronics, *M. Sankarapandian, P.K.C. Sripadarao, J. Fullam, M. Breton, R. Chao, S. Kanakasabapathy*, IBM Corporation, *A. Ko*, TEL Technology Center, America, LLC

Sub-Lithographic pitch patterning requires advanced patterning techniques capable of achieving reduced dimensions with current lithography technology. Novel techniques are employed to pattern gates with critical dimensions below the current resolution limits of optical lithography. One such technique is Sidewall Image Transfer (SIT), where the critical dimension of the gate is established by the controlled deposition of a spacer on top of a Lithographically defined mandrel. The material selection of the mandrel and spacer materials can influence the functionality of the SIT process, and this paper specifically compares the use of an ashable organic mandrel to an inorganic mandrel. Organic mandrels for mandrel removal selective surrounding spacer material. However inorganic mandrels, are resistant to profile modifications. In this paper, we compare both approaches with specific focus on the influence of plasma etch chemistries on mandrel profile characteristics.

9:20am **PS-MoM4 Trim Etch for sub-20 nm Technology**, ***Guangjun Yang***, *D. Keller, Y. Rui, R. Benson, A. Schrinsky*, Micron Technology

Photo resist trim with isotropic etch is a common practice in industry for CD control and line width roughness (LWR) improvement for sub 35 nm features imaged with 193nm lithography. As CD shrinks further, it becomes more challenging to control CD, to reduce line buckling or wiggling and to manipulate etch profile. For CDs below 20 nm, hardmask trim and live structure trim play an important role. In this talk, we will present a few examples of isotropic trim for sub-20 nm technology using mainly ICP chambers. In one case, DUV photo resist was trimmed from 40 nm to 15 nm with good LWR and good remaining height. In another case, a Si3N4/metal stack was trimmed down to 8 nm from 15 nm with good SWR (space width roughness) and etch profile. In the third case, we selectively trim DLC (diamond-like-carbon) in the bottom portion of the profile to make the etch profile straighter. Also we will discuss some challenges in developing a good isotropic trim process such as trim etch selectivity to materials and to location, etch uniformity. Finally we will discuss some opportunities for etch tool development.

9:40am **PS-MoM5 Laser-Assisted Dry Etch of poly-Si and SiO_2 for Semiconductor Processing**, ***Jason Peck***, *G.A. Panici, I.A. Shchelkanov, D.N. Ruzic*, University of Illinois at Urbana-Champaign

Dry etch assisted by laser (DEAL) of silicon and silicon dioxide via $Ar/SF_6/C_4F_8/O_2$ capacitively-coupled plasma was studied, with goals including form control for sub-22 nm features and uniformity for 450 mm wafer processes. The first phase of the work confirmed the feasibility of the proposed concept. The second phase of the work was focused on pulse frequency, length and wavelength influence on etching rate. Two lasers with different repetition rates, wave lengths and pulse widths were used. The first one is a (2.5 – 7 ns FWHM) Nd:YAG laser with repetition rate of 100 Hz. The Nd:YAG laser was capable to produce emission at 1064, 532 and 266 nm wavelengths. The second laser was a 1043 nm IMRA laser with 300 fs pulses and 1 MHz pulse rate. Continuous wave (CW) laser systems were also tested.

The etch rate enhancements were determined. The predominant laser-assisted etch mechanism was interpreted to be electrochemical, with electron-hole pairs catalyzing chemical etching at the surface. The influence of laser repetition rate was studied in both SF_6 and C_4F_8 etch. The beam intensity profile influence onto etch pattern was studied. In all cases, an emphasis on low power density kept the experiments well under the ablation threshold, minimizing pyrolytic damage by the incident beam. Impact on current industry processes will be discussed.

10:00am **PS-MoM6 Spatial Resolution Considerations for Uniformity Improvement by Gas Cluster Ion Beam Etch**, ***Joshua LaRose***, TEL Technology Center, America, LLC, *B. Pfeifer, V. Gizzo*, Tokyo Electron, *N. Joy, N.M. Russell*, TEL Technology Center, America, LLC

Abstract

Sub-14nm CMOS requires a demanding level of integrated thickness control at several critical layers in the fabrication process in order to meet functional and parametric yield/Cpk goals. Gas cluster ion beam (GCIB) etching is becoming increasingly adopted to meet this need by using precise corrective etching with location specific processing (LSP) to meet within-wafer and wafer-to-wafer control requirements. LSP etch correction may be driven by any input map delivered to the tool via factory automation, or may be driven by on-board integrated metrology. In either case the extent to which a uniformity pattern can be corrected may be limited by the length scale of non-uniform features as compared to the size of the beam, and the ability of the metrology sampling plan to resolve the features. Here we characterize in some detail, the influence of sampling density and non-uniformity length scale on LSP resolution capability.

LSP was able to substantially reduce the standard deviation of a model incoming non-uniformity map for features with > 8 mm length scale, and to adequately resolve such features, requires a metrology sampling plan corresponding to > 89 points on a 300 mm wafer. For wafer-edge non-uniformity, we show similar capability to resolve features > 10 mm by LSP, with sufficient metrology sampling density, and introduce a hybrid edge model scheme that can enable improved resolution of edge features with as few as 37 metrology points. Here we describe in detail the techniques used to determine the resolution performance, summarize results from several relevant cases, and present clear guidelines on sampling strategies for LSP etching.

10:40am **PS-MoM8 Analysis of Surface Reaction Layers formed by Highly Selective Etching with Pulsed Microwave Plasma**, ***Miyako Matsui***, Hitachi Ltd., Japan, *M. Morimoto, N. Ikeda, T. Ono*, Hitachi High-Technologies Corp. **INVITED**

Three dimensional (3D) transistors, such as a Fin-FET, have increasingly necessitated etching processes with higher selectivity and greater anisotropy. For example, a Si_3N_4 spacer layer needs to be anisotropically etched with a vertical profile without leaving residue on the sidewalls of the fins while keeping high selectivity in regard to Si fins. To provide more highly selective and more anisotropic etching for fabricating next-generation 3D devices, an etching system combining a pulsed-microwave ECR plasma and time-modulated wafer bias was developed.

In this study, the mechanism of highly selective etching with a pulsed-microwave ECR plasma was investigated by analyzing surface-reaction layers formed on etched materials. To clarify the etching mechanisms of poly-Si, Si_3N_4, and SiO_2, surface-reaction layers formed not only on unpatterned surfaces but also at the bottoms of line-and-space patterns were

analyzed by XPS. Specimens were etched using an $HBr/O_2/Ar/CH_4$ gas chemistry for poly-Si etching and using a $CH_3F/O_2/Ar$ gas chemistry for Si_3N_4 etching. The XPS results revealed that a modified layer formed on all etched materials and that a polymer layer formed on the modified layer. To determine the effects of the etching parameters on etching selectivity, the thickness and composition of the reaction layers, which were the polymer layer and the modified layer, were quantitatively analyzed. To examine the thermal reactivity between the reaction layers and the etched materials, etched surfaces were analyzed by TDS.

Highly selective etching mainly originated from the difference in the thickness of the polymer layers that formed on the etched materials under the pulsed plasma. The thickness of the polymer layer was controlled so that etching did not stop even at a low wafer bias voltage. Reactivity between the reaction layers and the etched material was controlled by adjusting the composition of the reaction layers. Especially in the case of Si_3N_4 etching, the N in the Si_3N_4 layer thermally reacted with the reaction layers, forming NH_3 or HCN, and the Si in the Si_3N_4 layer had high reactivity with the F in the reaction layers. Due to the high reactivity between the F-rich reaction layers and the Si_3N_4 layer caused by the pulsed plasma, the polymer layer became thin even at a low wafer bias and thus promoted ion-assisted etching. As a result, wide process windows were provided by formation of the reaction layers under the pulsed plasma.

11:20am **PS-MoM10 Improvement of Gate Shoulder Retention and SiN Selectivity over Si in Spacer Process**, ***Yohei Ishii***, *K. Okuma, N. Negishi, J. Manos*, Hitachi High Technologies America Inc.

To achieve improvements in semiconductor device performance, 3D transistors (FinFET) were introduced due to limitations in planar structures. Because of the complexity of the structure and high aspect ratio features, new challenges have appeared. Among many processes, spacer etch is one process that could have an impact on device performance. During spacer etch, there are several issues that arise such as SiN selectivity over Si and gate shoulder retention.

In this presentation, we will demonstrate a spacer etching process, using a novel gas, and utilizing a Hitachi microwave Electron Cyclotron Resonance (M-ECR) etcher. SiN selectivity over Si is improved compared to a conventional gas chemistry such as CH3F base process. In addition, while the spacer is etched, the gate shoulder has to be protected. Finally, we will also introduce an etching method that overcomes the trade-off relationship between gate shoulder retention and spacer etch.

11:40am **PS-MoM11 Advanced Patterning Applications Using High Selectivity Etch Chemistry**, ***Nathan Marchack***, *S.U. Engelmann, E.A. Joseph, R.L. Bruce, H. Miyazoe, E.M. Sikorski*, IBM T.J. Watson Research Center, *T. Suzuki, M. Nakamura, A. Itou*, ZEON Chemicals L.P., *H. Matsumoto*, Zeon Corporation, Kawasaki, Japan

Image reversal has been utilized in semiconductor manufacturing to invert line/space [US6221562 B1] and hole/pillar [US6358856 B1] patterns. Since this process requires the ability to remove one material with high selectivity to another, traditionally either contrasting dielectrics (such as SiN/SiOx) or complementary types of photoresist (e.g. positive/negative tone) have been used. While carbon-based soft materials are easier to deposit than dielectric films, lack of selectivity and physical integrity can potentially hinder successful image reversal processes when they are combined with hard materials, e.g. metals, dielectrics.

We present an image reversal process by depositing an organic planarizing layer (OPL) material into a hole array patterned in SiN to create pillars, which are a commonly required shape for a variety of emerging technologies. By using a gas chemistry with an extremely high selectivity to OPL, plasma etch removal of the SiN is possible, allowing pattern fidelity to be maintained at pitches below 100nm. We demonstrate control of the pillar CD by controlling the time of the OPL etchback step.

For applications requiring minimal mask budget, we utilize the same chemistry's selectivity to SiOx to demonstrate patterning of SiN hard mask features with reduced LER/LWR and iso/dense loading ratio. We demonstrate hard mask patterning of 80nm thick SiN with 35nm SiOx hard mask for 50nm pitch lines, with potential applications for advanced technology nodes. The results were achieved in both RLSA and ICP plasma sources.

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