Tuesday Morning, October 20, 2015

Materials Characterization in the Semiconductor Industry Focus Topic
Room: 114 - Session MC-TuM

Characterization of 3D structures
Moderator: Paul van der Heide, GLOBALFOUNDRIES, Inc.

8:00am **MC-TuM1 Expanding Roles of Materials Characterization and Metrology in Advancing Moore's Law**, *Z. Ma*, ***Ying Zhou***, Intel Corporation **INVITED**

Moore’s law scaling in the past decade was propelled by important technology breakthrough and innovation. Wide acceptance of popular low power devices such as smartphone and tablet continues to drive dimension scaling to achieve desired performance, power consumption and cost. However, traditional geometrical scaling for devices and interconnects encountered some fundamental material issues and scaling limits. To address these challenges, new classes of materials and device structures are being investigated for possible applications. The evaluation and introduction of disruptive process technologies and novel devices are driving strong interests in new material characterization techniques and methods. Process monitoring and control put stringent requirements on metrology capabilities at both technology development and manufacturing stages. This presentation will talk about the growing needs for materials characterization and metrology and their pivotal roles in enabling technology breakthrough and manufacturing sustaining. A comprehensive metrology approach is recommended to push ultimate analytical capabilities and accuracy while delivering required measurement consistency and data turns through automation and design for metrology.

8:40am **MC-TuM3 X-ray based Characterization of Strained SiGe on FinFETs**, ***Kriti Kohli***, *M.A. Smith, A. Madan, Z. Zhu, J.R. Holt*, GLOBALFOUNDRIES, *M. Klare*, Revera

The introduction of complex three-dimensional structures in device design presents challenges that require ever more sophisticated metrology with high accuracy and precision. One such example is the measurement of composition and thickness of epitaxially grown thin films on fins. Due to the preferential growth in the <111> plane of SiGe on fins, the film creates complex multi-faceted shapes on top of the fins. These 3D structures are challenging even for reference metrology to characterize due to the effects of shading and variability in geometrical area. The goal is to develop an inline metrology that measures composition and thickness of epitaxially grown SiGe directly on fins since blanket pads are no longer correlated to device performance. In this paper, we present a comprehensive characterization of a set of samples with varying geometry, thickness, strain and composition of SiGe films on fins using HRXRD, XPS, XRF and compare to reference metrology. With each technique, we have developed a methodology for measuring directly on 3D fins and compare the techniques to determine the most robust, precise and accurate metrology solution.

9:00am **MC-TuM4 Atomic Scale Analysis by Atom Probe on 3D Semiconductor Structures**, ***Ajay Kumar Kambham***, *S. Shintri, D. Flatoff, P. van der Heide*, Globalfoundries

Device structures are rapidly scaling down to the nanometer regime with the ongoing development in semiconductor device technology. Along with this, it is ever critical need to engineer dopant profiles and to define the formation of junctions in Metal-oxide field effect transistors (MOSFETs). This is increasingly challenging considering the severity of short channel effects (SCEs). Indeed, one type of SCE in MOSFET devices known to cause performance degradation is Drain Induced Barrier Lowering (DIBL). To reduce DIBL, dopant junction profiles are made more abrupt. This can be done through the introduction of Sigma/cavity structures and the modulation of stress through optimal engineered epitaxial buffer layers. To assess the quality over nanometer scale regions requires the use of analysis techniques such as Atom Probe Tomography (APT) and Transmission Electron Microscopy (TEM). This presentation will discuss the role of APT and how elemental distributions vary depending on type of faces employed, i.e. Si (100) vs Si (111) along with the challenges involved in sample preparation.

9:20am **MC-TuM5 Preparing and Characterizing Nanoscale Topological Insulators**, ***Kenneth Burch***, Boston College **INVITED**

Topological Insulators present new opportunities to control and manipulate spin in future nano-devices. A key difficulty has been realizing the rather high mobilities they promise and detecting unambiguous signatures of surface transport at high temperatures. I will discuss our groups efforts to prepare these materials on the nano-scale using mechanical exfoliation on various substrates with the aim of understanding the role of the substrate in their transport properties. In addition I will discuss the various optical probes (Raman and Infrared) we have applied to understand the phonons and their role in limiting the surface transport properties of these materials.

11:00am **MC-TuM10 ”More than Moore”: Could Silicene Be the Future of Electronics?**, *J. Avila, Ch. Chen, S. Lorcy*, ***Maria Asensio***, Synchrotron SOLEIL, France

For more than forty years, the miniaturization of circuits by scaling down the transistor has been the principal driver for the semiconductor technology. As the number of components per chip increases, the total chip size has to be reduced within workable limits. Consequently, the technology roadmap for semiconductors or ”Moore's Law”(1), which states that the number of components integrated in a circuit would increase exponentially over time, has been successfully achieved by a continuous downscaling of the critical dimensions in the integrated circuit. Hence, since 1970, the number of components per chip has doubled every two years. However, we are nowadays nearing the basic limits of the scaling, thus for further improvement we may need ”More than Moore”(2). This new attractive trend adds value to devices by incorporating more functionalities to them, which do not necessarily scale according to Moore’s Law. Graphene is one of the best-placed novel materials to be included in a ”More than Moore” approach. A close relative of graphene, a 2D honeycomb lattice of Si atoms called Silicene has been recently reported as nanoribbons and single layers on silver (111) oriented monocrystals, (3,4). As silicon, unlike carbon, prefers sp3 hybridization instead of sp2 hybridization, silicone possess several stable buckled structures, which are compatible with the opening of a small gap (5). This ability makes silicene very attractive to be integrated to the already well-developed silicon-based electronics.

The task to create a new ”fabric” as silicene has been, however, very difficult because silicene does not exist in Nature and it is not as easy to form as graphene due surely to its particular electronic structure and larger atomic size. Over the last decade, research groups from around the world have claimed to have prepared silicene, a one atom-thick layer of silicon. However, just recently our team has created silicone single sheets of silicon on silver single crystal surfaces and has further characterized this novel material; using atomic resolution STM spectroscopy and high-resolution angle resolved photoemission, proving unambiguously the existence of one of the most stable phases of this unique material. (3)

REFERENCES

(1) Moore G.E., Electronics, Electronics, 38, 8 (1965); reproduced

in Proc. IEEE, 86, 82 (1998).

(2) ITRS website, http://www.itrs.net/home.html

(3) P. Vogt, et al., Phys. Rev. Lett. 108, 155501 (2012)

(4) P. De Padova et al., Appl. Phys. Lett. 96, 261905 (2010)

(5) S.S. Cahangirov, et at., Phys. Rev. Lett. 102, 236804 (2009)

(6) S.S. Cahangirov, et at., Phys. Rev. B 90,(3) ,035448(2014)

11:20am **MC-TuM11 Challenges in Measuring Strain in Nanoscale 3D FinFET Structures**, ***Anita Madan***, GLOBALFOUNDRIES, *S. Mochozuki*, IBM Albany Nanotech Center, *C. Murray*, IBM, T. J. Watson Research Center, *D. Cooper*, CEA, LETI, MINATEC Campus, France, *Y. Wang, W. Weng, T. Pinto*, GLOBALFOUNDRIES

Strain engineering has been adopted as a key element for scaling high performance complementary metal-oxide-semiconductor (CMOS) devices. Complex 3D structures (FinFETs) have been introduced for the 14 nm technology node and beyond. Typically, strain is introduced by replacing the Si channel with SiGe for pFET devices. Characterization of strain in the fins is challenging due to the complexity of their three-dimensional geometries and their nanoscale dimensions.

In this paper, we present the methodology developed to characterize strain and crystallinity in both strained SiGe FinFET structures and FinFET structures with epitaxial embedded SiGe (eSiGe). We compare 2 complementary techniques used for characterization of strain on 3D fins. High Resolution X-ray Diffraction techniques with a spot size and a spatial resolution of 50 to 200 microns are non-destructive and the signal (averaged over many fins) is sensitive to defectivity, strain and Ge content. On the other hand, Transmission Electron Microscopy (spot size 0.3 – 5nm) is a destructive technique, dependent on the lamella thickness, and gives localized information on a few fins.

All measurements were made on blanket and fin array pads on specially designed macros. For XRD measurements, strain was evaluated using peak position information from the XRD Reciprocal Space Maps collected both parallel and perpendicular to the fin arrays. Measurements show that the stress in the SiGe fins is uniaxial – the SiGe fins are fully strained along the direction of the fins. The SiGe is partially relaxed perpendicular to the fins – the amount of relaxation dependent on the %Ge and the height of the SiGe fins. Advanced TEM analytical techniques (Nano beam diffraction, Dark Field holography and Energy-dispersive X-ray spectroscopy) were used to map the strain and %Ge over the height and the width of the SiGe fins. There was good correlation between the average strain and %Ge as determined from the TEM and XRD techniques. Results of the measurements will be compared with theoretical modeling, which is used to quantify the triaxial stress tensor components based on the experimentally determined lattice parameter values.

The advent of new HRXRD tools with 1D detectors and high intensity sources enable these measurements to be made over a couple of hours. Since XRD techniques are non-destructive, we will also discuss how this methodology can be easily adapted as in-line metrology to monitor the change in strain with processing.

This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities.

11:40am **MC-TuM12 Strain Measurement using Electron Beam Techniques**, ***Jean-Luc Rouviere***, CEA-University Grenoble Alps, France, *N. Bernier*, CEA, LETI, MINATEC Campus, France, *D. Cooper*, CEA-LETI, France **INVITED**

Strain can modify deeply material properties such as optical emission, transport properties or structural strength. With the development of nanotechnologies, the need of tools that can measure strain with high accuracy (about 0.01%) and high spatial resolution (about 1 nm) has appeared. The demand of Microelectronics industry has been particularly strong since Intel has implemented strained channels to boost the transport performance of their devices, and during the last decade, many new TEM base techniques have been developed to reach these goals. Of course, not only the microelectronics industry, but also any fields involving nanomaterials will benefit from these developments.

In this presentation, after a short review of the different TEM techniques, we will focus on the solution we have developed and chosen: **Nanobeam Precession Electron Diffraction (N-PED**). Like in all TEM diffraction techniques, a small electron beam is made and diffraction patterns are acquired at different positions of the electron beam. In addition, in N-PED, the incident electron beam is rotated by a small angle around the observation direction and a descan is applied after the sample in order to bring back the diffracted beams to their unprecessed positions. In fact there is a compromise between spot size, beam convergence and precession angle. We adopted a setting where the beam convergence is about 2.2 mrad, the probe diameter is of about 1 nm, and the precession angle is below 0.5°. The advantages of this setting for strain measurement are mainyfold : (i) the diffraction spots have disk shapes and do not saturate, (ii) the intensity within the diffraction disks is more uniform (iii) more diffraction disks are visible (iii) a greater accuracty is obtained by locating the edges of the disks, (iv) the measurements are very stable versus changes in sample thickness or orientation and (v) strain maps of 4 components of the 3D strain tensor can be obtained with one zone axis orientation. **We will show how this simple and robust N-PED technique has been used successfully for the analysis of microelectronics devices and nanostructures**. In our FEI TITAN ultimate microscope where we used a Gatan Ultrascan CCD camera, the main drawbacks of N-PED are (i) its relatively slow speed and (ii) the amount of stored data to acquire large maps. For instance, to acquire 100x50 diffraction patterns containing 1Kx1K pixels, it took 90 minutes and 12 Gbytes on the hard disk. However with the new available fast cameras and larger disks, these issues are greatly reduced.

Authors Index

Bold page numbers indicate the presenter