Electronic Materials and Processing
Room: 210E - Session EM-WeA

Interconnects: Methods and Materials for Removing Connectivity Constraints
Moderator: Andy Antonelli, Nanometrics, Michelle Paquette, University of Missouri-Kansas City

2:20pm **EM-WeA1 Interdiffusion Characterization of Selective Chemical Vapor Deposition Cobalt Cap and Copper**, ***Jeff Shu***, *Z. Sun, S. Choi, B. Yatzor, Z. Bayindir, G. Zhang, Y. Lee, H. Liu, J. Lansford*, GLOBALFOUNDRIES U.S. Inc.

Electromigration (EM) failure is always one of the key challenges of BEOL Cu interconnects. The continuous shrink of Cu feature size leads to higher current densities, which lower EM lifetimes. The interface between Copper and dielectric cap has been identified as the key diffusion path for copper atoms, and the adhesion of the interface is critical to EM performance. Different methods developed to improve the adhesion between copper and dielectric cap interface. One method of improving the adhesion has been the use of alloy seed, CuMn or CuAl. Mn (Al) will segregate and bond chemically to the copper and dielectric cap interface during dielectric cap deposition which can improve the adhesion of the interface and suppress Cu atoms migration along the interface under current stress. An alternate method of improving the adhesion is to have a self-aligned CoWP Cap or Selective CVD Co Cap on top of Cu which was developed for more stringent EM requirement of advanced nodes, such as 32nm, 20nm and beyond. Compare to self-aligned CoWP plating process, selective CVD Co Cap has higher selectivity and more compatible with porous ultra low k film. In this paper, we focus on interdiffusion characterization of selective CVD Co cap and copper. Co/Cu interdiffusion of cobalt films with different precursors are thoroughly evaluated and compared. Nitrogen content in Co film which enriches the grain boundaries due to low solubility in Co was identified as the key knob to control Co/Cu interdiffusion. Less nitrogen in Co film results in more copper diffusion. Better EM results on 20nm groundrule test structures demonstrated with higher nitrogen in Co film. Thermal anneal with H2 gas was found to be able to reduce nitrogen content in Co film which result in more Cu diffusion. Secondary Ion Mass Spectrometry (SIMS), X-ray photoelectron spectroscopy (XPS) and Electron Energy Loss Spectroscopy (EELS)/ Energy Dispersive X-ray Analysis (EDX) line scan were used for Cu diffusion characterization which clearly show Cu signal on top of Co film. A novel analytical technique of SIMS has been developed to characterize nitrogen content in Co film that CoN was selected as nitrogen detection molecular since nitrogen has some interaction with Co within the film.

2:40pm **EM-WeA2 Contact Engineering on Carbon Nanotube Interconnect Vias**, ***Yusuke Abe***, *A. Vyas, R. Senegor, C. Yang*, Santa Clara University

Nanocarbons such as carbon nanotubes (CNTs) and graphene are candidate materials for next-generation integrated circuit technologies due to their high current-carrying capacities and excellent electrical, thermal, and mechanical properties [1,2]. The key performance-limiting factor continues to be the high contact resistance at the interface with metal electrodes [3]. Metal depositions are frequently used during post-fabrication contact engineering for these nanocarbons to mitigate the high resistances between these materials and metal electrodes, with various degrees of success in achieving stable low-resistance contacts [4]. We have fabricated test devices for CNT vias, and measured their current-voltage (I-V) characteristics [5]. In this study, post-fabrication contact engineering is performed using electron-beam induced deposition of tungsten (EBID-W) [6] to improve the electrode contacts and hence reduce the total device resistance.

Fabrication of these via test structures without top contact metallization was described elsewhere [5]. In the present study, EBID-W is used to form the via top contacts (Fig. 1). From I-V and resistance measurements on 500 nm x 500 nm CNT vias with and without EBID-W top contact metallization, the effect of EBID-W contact on resistance reduction is clearly demonstrated (Fig. 2). While similar improvement can be obtained by current stressing without contact metallization [5], such technique would introduce an additional thermal cycle to the chip fabrication process and hence undesirable. On the other hand, the resistance of a via with W top contact is shown to have reached its minimum which is unaffected by further annealing (Fig. 3). Thus the contact resistance of the CNT via is indeed improved by top contact metallization with W, and that the resistance is stable. Without increasing the thermal budget from current stressing in chip fabrication, the use of EBID-W for via top contact metallization could facilitate the eventual functionalization of CNT via interconnects.

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3:00pm **EM-WeA3 Innovative Technological Solutions for Low-k Integration Beyond 10 nm**, ***Mikhail Baklanov***, IMEC **INVITED**

The general issue of porous low-k materials is degradation of their properties with the increasing porosity. The porous materials are soft, mechanically weak, and do not adhere well to silicon or metal wires. The large pore size also make them more sensitive to plasma damage (because of easy penetration of plasma species into the pores). All these challenges are becoming critical in advanced technology nodes when the distance between the metal wires has reduced to tens nm. This is the reason why the present efforts of researches and engineers are oriented to development and evaluation of new types of low-k materials. The materials need to have good mechanical properties, to have sufficient chemical and plasma resistance and small pore size. At the same time the research efforts are also oriented to development of new technological approaches reducing degradation of low-k materials during the integration. The invited talk will include 2 parts. 1. The first part of presentation includes the results of evaluation of new materials with low dielectric constant that are considered as potential candidates for future generations of nanoelectronic devices. These dielectric materials includes new generations of organosilicate glasses (Periodic Mesoporous Organosilicates (PMO), Zeolites and Metal-Organic Frameworks (MOFs). Fabrication of PMO materials is based on self-assembling chemistry and therefore it allows better control of critical properties of low-k materials. MOFs and Zeolites have very small pore size and unique mechanical properties. These materials have been developed in collaboration with several Universities. Their evaluation at imec includes measurement of their porosity and pore size (ellipsometric porosimetry – a technique patented by author), mechanical properties using Nanoidentation, chemical composition (FTIR, XPS, SIMS and some other techniques). Dielectric constant of these materials are measured my using metal-insulator-semiconductor (MIS) structures with Pt electrode. 2. The second part of the presentation is related to development of innovative technological approaches that are considered as key solutions for successful integration of porous low-k materials. Particularly, detailed analysis of recently patented cryogenic plasma etching of low-k materials will be reported. In this technology, the initial chemistries and reaction products are condensed in pores, makes the material dense and prevent penetration of plasma active into the bulk of low-k materials and reduce the plasma "damage". The results of evaluation have already been published in several papers. By using this technique the lowest integrated k-value of ultralow-k material has been achieved. Completely different integration scenario is considered for 5 nm technology nodes. The damascene technology can't work in this case because of plasma damage of low-k and the technology can return back to the subtractive approach with metal patterning. Although some industrial Companies are trying to develop technology of plasma etching of Cu, we are developing an alternative approach with metal patterning by using patterned sacrificial polymers. After metal deposition and planarization by chemical mechanical polishing , the sacrificial polymer is removed by using hydrogen plasma, then the trenches and vias are filled by ultralow-k dielectrics. The deposited low-k films is not exposed to plasma. The first results have been generated, the dielectric constants were achieved close to ones obtained cryogenic etch technology. However, some challenges still remain and they also will be highlighted.

4:20pm **EM-WeA7 Challenges and Directions for Dielectric Interconnect Materials for the 10nm node and Beyond**, ***Jeffery Bielefeld****, J. Blackwell, S. Bojarski, M. Chandhok, J. Clarke, C. Jezewski, N. Kabir, S.W. King, M. Krysak, D.J. Michalak, M. Moinpour, A. Myers, J. Plombon, M. Reshotko, K. Singh, J. Torres, R. Turkot, H. Yoo*, Intel Corporation **INVITED**

To enable the continued scaling of interconnect layers for the 10nm node and beyond an increased number of materials and integration challenges will need to be addressed. Historically, interconnect dielectric materials have been broken down into Interlayer Dielectrics (ILDs) and Etch Stop (ES) / Hard Mask (HM) materials. The ILD layer is the major driver in capacitance improvement, while the ES layer enables patterning and acts as a diffusion barrier. In this paper, we will discuss two major challenges: (1) Pathways for the integration of porous low-k ILDs, and (2) Development needs for ES materials to enable improved patterning options.

The industry continues to work on the integration of low-k ILDs, but the momentum to implement these films has slowed in recent years due to the challenges of working with porous thin films. Low-k ILDs (k~2.0) exhibit 40-50% porosity with an interconnected pore network. The increased porosity can lead to damage and increased roughness during patterning, and can allow precursor penetration during the metal barrier deposition. To mitigate the problems of integrating a porous ILD, we have utilized the approach of pore stuffing. In this process, a sacrificial material is infiltrated into the pores of a fully cured ILD. The resultant film is non-porous with increased mechanical properties.

In this paper, we will discuss the challenges of finding a pore stuffing material that can fill the pores of the ILD, remain in place during dual damascene processing and can then be removed from the low-k ILD post metallization and CMP. In addition, we will show how pore stuffing improves trench profiles, and how it prevents metal penetration during barrier deposition. Finally the successful implementation of this process will be demonstrated and integrated capacitance improvement will be presented.

In a classic dual damascene flow, the ES layer is used as a diffusion barrier and as a patterning stop between ILD layers. To enable more advanced patterning and integration schemes, the role of these materials needs to be expanded. Specifically, there may be situations where multiple ES/HM materials are needed and with high etch selectivity to each other (>20:1). Etch selectivity values for typical materials (e.g. nitrides, carbides, amorphous silicon, metal hard masks and carbon hardmasks) are not currently sufficient. Development of new material options, deposition techniques and etch processes are needed. In this paper, we will discuss the current needs for new ES\HM materials and novel etch technology, along with our current progress toward this challenge.

5:00pm **EM-WeA9 Pore Sealing of Low-k Films by UV Assisted CVD Processes**, ***Priyanka Dash****, D. Padhi*, Applied Materials

Porous ultra-low k (ULK) dielectric films with high porosity and larger pore size (k<2.4 and beyond) pose a serious challenge for their integration into next-generation microchips. In this paper, we report the formation of a thin layer of SiCxNy based pore sealing film deposited by UV assisted CVD. This film when deposited on damaged ULK surface assists in sealing the interconnected pores to prevent diffusion of metal liner and barrier metal precursors during the subsequent metallization steps. In addition pore sealing also enables an efficient sidewall protection to ULK thereby reducing its degradation by radical penetration during subsequent wet clean processes. A side benefit of this method is replenishment of depleted methyl species in damaged subsurface sites thereby improving hydrophobicity and recovery of k damage. A very thin pore seal film ~15 Ang is found to be sufficient to prevent metal precursor diffusion into a porous ULK k2.4 material. Porosimetry and backside SIMS were used to assess sealing behavior on surface pores of damaged ULK. On pattern wafers pore sealing treatment has been shown to significantly improve VBD and TDDB of k2.4 ULK to a level comparable to that observed for industry standard ULK k2.55 material. No structural change is observed in pattern CD for up to 15A of pore-seal deposition. Although this deposition is highly selective to surface sites available on damaged ULK, a thin layer (i.e. < 5A) of pore seal residue formed on Cu via bottom has been shown to be completely removed by typical CuOx wet clean solutions. Kelvin via measurements on structure wafers show that pore-seal with wet clean yields comparable via resistance as compared to wafers without pore-seal.

5:20pm **EM-WeA10 Copper Deposition and *In Situ* Chamber Cleaning using Pulsed-CVD Technique**, ***Fabien Piallat****, J. Vitiello*, Altatech, France

Due to the conformity required for deposition of metals in high aspect ratio vias, Physical Vapor Deposition is replaced by techniques from the Chemical Vapor Deposition (CVD) family. Conformity wise, the Atomic Layer Deposition (ALD) appears to be the best of the CVD techniques, but the low throughput is dissuasive for layers thicker than 10nm. At the edge between CVD and ALD, the Fast Atomic Sequential Technique (FAST) developed and patented by Altatech, enables deposition of layers with conformity close to the ALD at a higher throughput.

Through Silicon Vias are extensively used for interconnections and necessitate highly conductive materials in holes of aspect ratio higher than 10. Of all low-resistivity metals, namely Ag, Al, Au, Cu and W, studies showed that Cu is the best for filling trenches. Therefore, both the metal and the technique used are imposed, i.e. Cu deposition by CVD is the most suitable solution.

The main obstacle for a complete adoption of Cu as an interconnection metal is the difficulty to clean the chamber after process, since Cu cannot be etched by the usual fluorinated in-situ dry etching processes.

Successful deposition of conformal Cu layer was performed in vias with an aspect ratio of 10, using Altatech AltaCVD deposition chamber and a commercially available Cu precursor. Optimised deposition parameters resulted in low resistivity Cu, down to few µΩ.cm, with deposition rates higher than 100 $nm.min^{-1}$. Plotting the deposition rate depending on the substrate temperature highlighted an Arrhenius law behaviour, which in turn provided the optimal deposition temperature. Complementary SEM observation showed Cu layer with low roughness.

Futhermore, taking advantage of the Altatech pulsed solution, FAST, an in-situ dry cleaning process was developed using hexafluoroacetylacetone (hfacH) solvent. The main scheme for Cu etching comprise one step of Cu surface oxidisation and a second step where CuO_x compounds react with hfacH solvent to form volatile species. Several approaches were assessed; the following one will be presented and discussed:

O_2 and hfacH introduced simultaneously in the chamber

Alternation of O_2 plasma and hfacH fill

Pulsed alternation of O_2 and hfacH fill

O_2 plasma and pulses of hfacH

Optimising and understanding the influence of each process parameter was made possible by the use of a Residual Gaz Analyzer (RGA) and an Optical Emissions Spectrometer (OES). Cleaning efficiency at the particle generation level of all the approaches are compared, after few microns of Cu deposition and a chamber clean.

Finally, the efficiency of the most promising approach will be investigated on different chamber coatings.

5:40pm **EM-WeA11 Study of UV Impact on PECVD Non-Porogen ULK (Ultra low κ) SiCOH Film Nano-Structures, Film Mechanical and Electrical Properties**, ***Zhiguo Sun****, J. Shu, S. Srivathanakul, H. Liu*, GLOBALFOUNDRIES U.S. Inc.

With the continuous shrinkage of back end of line (BEOL) metal pitches of sub-10nm technology node, integration with ultra-low κ (ULK) film becomes even more challenging. In comparison to traditional PECVD ULK films introduces pore through deposition with porogen precursor followed by UV or E-beam exposure to generate porosity , a new single precursor based ULK (ultra low κ) film has been formed without porogen and show promising on the sub 10nm technology road map . In this paper, we will use transmission Fourier Transform-Infrared (FTIR) spectroscopy, X-ray photoelectron spectroscopy (XPS) and Ellipsometric Porosimetry (EP) etc. to investigate the impact how different UV conditions will modify chemical bondings, film composition, pore structure and porosities. The role of UV in this new type of ULK film formation will be studied while difference UV conditions include UV bulbs and UV curing vacuum ambient etc. Film mechanical properties as well as electrical properties will be thoroughly compared. The interaction with downstream integration process steps, such as plasma induced damage and selectivity to MOCVD cobalt capping will be examined.

6:00pm **EM-WeA12 Bandgap Narrowing in Low-K Dielectrics**, ***Xiangyu Guo****,* University of Wisconsin-Madison*, S.W. King,* Intel Corporation*, P. Xue,* University of Wisconsin-Madison*, J.-F. de Marneffe, M. Baklanov,* IMEC, Belgium*, V. Afanas'ev,* Catholic University of Leuven, Belgium*, Y. Nishi,* Stanford University*, J.L. Shohet*, University of Wisconsin-Madison

Electrical reliability in Cu interconnect structures has become a vital concern as the nano-electronics industry moves to sub-16 nm technology nodes and strives to implement insulating dielectric materials with increasingly lower dielectric constants (i.e., low-k). Studies have shown a direct correlation between trap/defect densities and electrical leakage of low-k materials,[1,2] , while the knowledge of the fundamental mechanism producing the damage is still limited. The bandgap energy, often serving as a reference point from which the presence and location of defect states in the bulk or at the interface can be understood, is of fundamental importance for understanding the electrical degradation in these dielectrics. In this work, core-level X-ray photoelectron spectroscopy (XPS) was utilized to

determine the surface bandgap for various non-porous and porous low-k a-SiCOH dielectrics before and after ion sputtering by examining the onset of inelastic energy loss in core-level atomic spectra. Bandgap narrowing was observed in Ar+ ion sputtered low-k dielectrics. The reduction of bandgap energies ranges from 1.3 Ev to 2.2 Ev depending on the film composition. By examining the valence-band spectra measured with high-resolution XPS, we show that the bandgap narrowing in the low-k dielectrics is contributed to the arising and uplifting of the valence-band tail as evidenced by the presence of additional electronic states above the valence-band maximum (VBM). Electron spin resonance (ESR) measurements were also performed on the a-SiCOH films and the localization of each type of defect within the dielectric band gap is analyzed and compared. A combination of these results with the band gap measurements suggests the additional electron states contributing to the narrowed bandgap originate from carbon-related defects in the material. This work was supported by the National Science Foundation under Grant CBET-1066-231 and by the Semiconductor Research Corporation under Contract 2012-KJ-2359.

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