Electronic Materials and Processing
Room: 210E - Session EM+NS+PS-MoM

More Moore! Materials and Processes to Extend CMOS Another Decade

Moderator: Christopher Hinkle, University of Texas at Dallas

8:20am **EM+NS+PS-MoM1 Effects of Deposition Temperature and Pre-rapid Thermal Process on Electrical and Interfacial Characteristics of Alumina on GaSb**, ***Seongkyung Kim***, *H.J. kim*, Seoul National University, Korea, Republic of Korea

Recently Ⅲ-Ⅴ compound materials have attracted significant attention as promising channel materials for sub-10 nm logic MOSFET due to their high mobility. GaSb is a strong candidate for pMOSFETs because of its high hole mobility in addition to the insolubility of its native oxides. Even with the outstanding electrical properties of GaSb, there are some drawbacks related to the instability of its native oxides and metallic layer of elemental Sb. The native oxides and metallic layer of elemental Sb are considered to be sources of Fermi level pinning and flat C-V curves. Therefore, it is necessary to improve surface treatment methods. Since it is possible to eliminate its native oxides and elemental Sb by heating them, it is essential to research temperature related surface treatments.

In this study, various ALD temperatures from 190 ºC to 310 ºC and pre-RTP(Rapid Thermal Process), which is first introduced here as a pre-deposition treatment, have been adopted for eliminating the remaining native oxides after cleaning. N_2 gas atmosphere is used to suppress the oxygen to interact with GaSb surface for the pre-RTP. GaSb metal-oxide-semiconductor capacitors were fabricated on p-type GaSb, which has a carrier concentration of 1.0~2.0 x 10^{17} cm^{-3}. GaSb was degreased with acetone, ethanol, and isopropane for 5 minutes each and then etched by HCl. 10 nm of Al_2O_3 has been deposited as a gate dielectric with TMA and DI water by thermal ALD. For the metal gate, a Pt electrode has been deposited with an electron-beam evaporator.

When the deposition temperature increases, the Ga_2O_3 peak increases and the substrate peak decreases under XPS analysis. It is observed that the amount of Sb increases at the GaSb/Al_2O_3 interface as the deposition temperature increases in AES depth profiles. Both Ga2O3 and elemental Sb have increased generation as the deposition temperature increases, since the surface chemical reactions are accelerated by increased temperature. The CV curve becomes flat as the deposition temperature increases. It indicates that Ga_2O_3 has a flattening effect of the CV curve and the more amount of Ga_2O_3 that is generated, the flatter the CV curve will become.

Desorption of the native oxides and elemental Sb should occur by annealing the substrate. After the pre-RTP, the amount of elemental Sb increases, since the remaining native oxide, after cleaning, is reduced by increased temperatures. The remaining native oxide Sb_2O_3, after cleaning, supplies oxygen to the substrate and becomes elemental Sb. The leakage current increases with pre-RTP. It shows that the elemental Sb increases the leakage current. Further study on optimizing pre-RTP conditions is needed.

8:40am **EM+NS+PS-MoM2 Selective Wet Etching of III-V Semiconductors with HCl and H_2O_2**, ***Pablo Mancheno-Posso***, *. Jain, A.J. Muscat*, University of Arizona

The etching of III-V semiconductors is needed to insert these materials into current device flows to extend CMOS transistor technology. III-V oxides are detrimental to electrical performance and must be removed, because they adopt different oxidation states and can be soluble in water. Plasma etching to create profiles can damage and change the stoichiometry of the surface. Wet etching of these oxides can control the roughness and chemical termination of the surface by choice of oxidant and etchant, concentration, and pH. Wet etching of III-V semiconductors is accomplished by oxidizing acid and base chemistries that can preferentially remove group III or V atoms. In new 3 D transistor architectures, the formation of the channel fin requires a low etching rate to ensure a smooth surface and a highly selective etching bath with respect to other materials or crystal faces that are exposed. In this work, we varied the group III and V atoms across five binaries (GaAs, InAs, InP, GaSb, and InSb) and measured etching rates. These materials were etched using mixtures of HCl (0.01 M) and H_2O_2 (0.0001-5 M). The etching rate was measured using profilometry on wafers patterned with conventional photolithography. The chemical composition was monitored using X-ray photoelectron spectroscopy (XPS). The etching rate of GaAs and InAs (same group V atom) exhibited a volcano-shaped dependence on H_2O_2 concentration. At H_2O_2 concentrations of 5 to 100 mM, the etching rate increased linearly from 0.08±0.03 to 1.1±0.1 nm/s for GaAs and from 0.06±0.04 to 0.9±0.3 nm/s for InAs. The rate decreased to 0.04±0.01 nm/s for GaAs and 0.26±0.13 nm/s for InAs at 1 M H_2O_2. InP, which is often exposed during etching of another III-V, showed a linear dependence on H_2O_2 concentration (0.01 to 5 M), increasing from 0.003±0.001 to 0.012±0.009 nm/s. The selectivity of etching GaAs to InP at three points along the volcano was about 55, 140, and 4 at H_2O_2 concentrations of 0.01, 0.1, and 1 M. Like the arsenides, the antimonides etched at about the same rate, but the volcano dependence moved to lower peroxide concentrations. The etching rate of GaSb increased from 0.07±0.04 to 0.21±0.04 nm/s and InSb from 0.09±0.03 to 0.38±0.09 nm/s for H_2O_2 concentrations from 0.1 to 1 mM. The group V atom determined the etching rate and is involved in the rate determining step in the reaction. The presence of As-Cl bonds on the surface after etching GaAs in HCl was confirmed by temperature programmed desorption (TPD) experiments after immersion in 1.7 M HCl. The mechanism for etching III-V semiconductors will be discussed based on the etching rate data and chemical composition of the surface.

9:00am **EM+NS+PS-MoM3 Border Trap Analysis and Reduction for ALD High-k InGaAs Gate Stacks**, ***Kechao Tang***, Stanford Univ., *R. Winter*, Technion – Israel Inst. of Tech., *T. Kent*, UC, San Diego, *M. Negara*, Stanford Unive., *R. Droopad*, Texas State Univ., *A.C. Kummel*, UC, San Diego, *M. Eizenberg*, Technion – Israel Inst. of Tech., *P. McIntyre*, Stanford Univ.

For future high performance III-V n-channel MOS devices, $In_{0.53}Ga_{0.47}As$ is a promising material for the channel due to its high electron mobility. Atomic layer deposited (ALD) Al_2O_3 has a large conduction band offset to InGaAs and can form a low defect-density interface with InGaAs [1]. ALD-HfO_2 can achieve a very low EOT (effective oxide thickness) with low gate leakage [2]. Therefore, both of these oxides have received extensive attention as candidate dielectric layers for InGaAs nMOSFETs. Apart from the well-known oxide/InGaAs interface charge traps that may pin the Fermi level of the channel, traps in the oxide layer, called border traps, may also reduce the charge in the channel and thus degrade the on-state performance of InGaAs MOSFET devices. We report a study of the effects of various approaches to reduce the density of border traps (N_{bt}), such as variation of the ALD temperature, and of post-gate metal forming gas (5% H_2/95% N_2) anneal (FGA) conditions.

Experimental methods employed include quantitative interface trap and oxide trap modeling [3, 4] of MOS capacitor data obtained over a range of frequencies and temperatures. We find that MOS capacitors fabricated using trimethylaluminum (TMA)/H_2O at an ALD temperature of 120°C have a considerably lower border trap density while maintaining a low interface trap density (D_{it}) compared to samples prepared with a more standard 270°C Al_2O_3 ALD temperature. It is also found that large-dose (~6,000 L) exposure of the $In_{0.53}Ga_{0.47}As$ (100) surface to TMA immediately after thermal desorption of a protective As_2 capping layer in the ALD chamber is an important step to guarantee the repeatability of high quality Al_2O_3/InGaAs samples made at Al_2O_3 ALD temperatures much lower than 270°C. The reduction of N_{bt} is consistent with time-of-flight secondary ion mass spectrometry depth profiles that show more effective hydrogen incorporation in the low-temperature ALD-grown Al_2O_3 films during post-gate FGA.

The N_{bt} of Al_2O_3 under various conditions will be compared with that of low-temperature ALD-grown HfO_2 films on InGaAs substrates. For the HfO_2 case, we also confirm the independence of border trap response on the electrical measurement temperature and check the influence of the crystal orientation of the InGaAs surface on MOS interface characteristics.

This work was supported by the US-Israel Binational Science Foundation.

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[2] V. Chobpattana et al., J. Appl. Phys. 114 (2013), 154108

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9:20am **EM+NS+PS-MoM4 Self-LIMITING CVD of an Air Stable Silicon Oxide Bilayer for Preparation of Subsequent Silicon or Gate Oxide ALD on InGaAs(001)-(2x4)**, ***Mary Edmonds***, *T. Kent, S. Wolf*, University of California at San Diego, *J. Kachian, N. Yoshida, M. Chang*, Applied Materials, *D. Alverez*, Rasirc, Inc, *R. Droopad*, Texas State University, *A.C. Kummel*, University of California at San Diego

A broader range of channel materials allowing better carrier confinement and mobility could be employed if a universal control monolayer (UCM) could be ALD or self-limiting CVD deposited on multiple materials and

crystallographic faces. Si-OH is a leading candidate for use as the UCM, as silicon uniquely bonds strongly to all crystallographic faces of $InGa_{1-x}As$, $In_xGa_{1-x}Sb$, $In_xGa_{1-x}N$, SiGe, and Ge enabling transfer of substrate dangling bonds to silicon, which may then subsequently be functionalized with an oxidant such as HOOH(g) in order to create the UCM terminating Si-OH layer. This study focuses on depositing a saturated Si-OH seed layer on InGaAs(001)-(2x4) at a substrate temperature of 350°C. XPS in combination with STS/STM were employed to characterize the electrical and surface properties of the saturated Si-OH seed layer on InGaAs(001)-(2x4).

The 350°C self-limiting CVD procedure includes a decapped $In_{0.53}Ga_{0.47}As(001)$-(2x4) surface dosed with total 87.6 MegaLangmuir Si_2Cl_6 followed by 210.55 MegaLangmuir total anhydrous HOOH(g). Complete saturation of silicon coverage is determined to occur once further dosing with Si_2Cl_6 leads to no further increase in the silicon 2p or further decrease in the substrate gallium 3p peak areas. Complete surface saturation of Si-O_x on InGaAs(001)-(2x4) was determined to occur once no further increase in the O 1s peak was seen with additional anhydrous HOOH(g) doses. Following Si-OH surface saturation, 300,000 L TMA was dosed at 250°C, and XPS shows the emergence of Al 2p and C 1s peaks indicative of TMA surface nucleation. The surface was then dosed with 500 L atomic H at 250°C to remove the methyl groups on the surface aluminum and replace with -H termination as well as remove any residual chlorine left on the surface. The surface was then exposed to air for 30 minutes, dosed with an additional 500 L atomic H at 250°C, and then STS measurements were performed. STM measurements of the Si-O_x surface show uniform surface coverage. STS measurements show the surface Fermi level position moves towards midgap due to a surface dipole formation from –OH groups and oxygen bonding to the surface. TMA dosed on the Si-O_x surface shifts the Fermi level back towards the conduction band, consistent with unpinning and the -OH induced surface dipole being lessened through surface bonding with dimethylaluminum groups. Following hydrogen dosing and air exposure, the surface Fermi level remains near the conduction band edge consistent with the surface being stable and unreactive in air. Preliminary MOSFET studies on InGaAs(001) show equivalent performance with Si_2Cl_6 predosing compared to in-situ cleaning with atomic H.

9:40am **EM+NS+PS-MoM5 Going Big in Two-Dimensions**, ***Joshua Robinson***, The Pennsylvania State University **INVITED**

The last decade has seen nearly exponential growth in the science and technology of two-dimensional materials. Beyond graphene, there are a variety of layered materials that provide a broad range of electronic characteristics useful for transistors, flexible electronics, sensors, and photodetectors, to name a few. However, bridging the gap between science and teechnology often lies in one's ability to synthesize materials on the wafer scale (or bigger). In this talk, I will discuss recent breakthroughs for direct growth of two-dimensional atomic layers and heterostructures with scalable techniues such as metal-organic chemical vapor deposition. We have demonstrated the direct growth of MoS_2, WSe_2, MoS_2/WSe_2, and hBN on epitaxial graphene to form large area van der Waals heterostructures. We reveal that the properties of the underlying substrate dictate properties of the layers and heterostructures, and that the direct synthesis of TMDs on epitaxial graphene exhibits atomically sharp interfaces. Our work has lead to a better understanding of vertical transport in 2D heterostructures, and we have identified new phenomenon in multi-junction heterostructures that has lead to resonance tunneling between layers and ultimately negative differential resistance.

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10:40am **EM+NS+PS-MoM8 2D Bipolar Devices for Novel Logic Applications: Fabrication, Characterization and Applications**, ***Ji Ung Lee***, SUNY Polytechnic Institute **INVITED**

The three pillars in semiconductor device technologies are (1) the p-n diode, (2) the MOSFET and (3) the Bipolar Junction Transistor (BJT). They have enabled the unprecedented growth in information technology that see today. For any new material, therefore, the development of these three devices is critical for providing benchmark performance against highly scaled Si-based technologies. Here, we will describe our efforts to fabricate and characterize these three benchmark devices in 2D materials, including graphene and transition metal dichalcogenide semiconductors (TMDs).

Although graphene is gapless, we will describe device concepts based on graphene p-n junctions that can lead to steep subthreshold slope devices. Critical to realizing such devices is the demonstration of relativistic Klein tunneling, a property of chiral carriers that arise from the unique electronic structure of graphene. Here, we will describe the fabrication and characterization of graphene p-n junctions, and discuss the unique tunneling properties that arise in these junctions and our efforts to realize high efficiency switching devices.

Using TMD materials, we have fabricated a single device that can reconfigure into p-n, MOSFET, and BJT devices. The reconfigurable device allows us to provide fundamental linkages between material properties and device performance not possible by fabricating the three devices individually. We will provide our method of fabrication and describe electrical and optical properties of the reconfigurable device.

11:20am **EM+NS+PS-MoM10 Electron Transport and Tunneling in Graphene-based Heterostructures**, ***Emanuel Tutuc***, The University of Texas at Austin **INVITED**

Vertical heterostructures consisting of atomic layers separated by insulators can open a window to explore the role of electron interaction in these materials, otherwise not accessible in single layer samples, as well as to explore device applications.

We describe here the realization of vertical heterostructures consisting of graphene, hexagonal boron nitride (hBN), and transition metal dichalcogenides realized using a layer-by-layer transfer. In double bilayer graphene heterostructures separated by hBN dielectric [1] where the two layers are rotationally aligned the interlayer tunneling current measured as a function of interlayer bias reveals a gate-tunable resonance thanks to momentum conserving tunneling. [2, 3] We discuss potential device application based on these experimental observations, as well as metrics that allow a benchmarking of their performance.

We also discuss the realization and characterization of graphene-MoS_2 heterostructures, which reveal a strong negative compressibility in the MoS_2 layer as a result of electron-electron interaction. [4]

Work done in collaboration with Kayoung Lee, Babak Fallahazad, Sangwoo Kang, Stefano Larentis, Hema C. P. Movva, Sanjay K. Banerjee, Leonard F. Register, Takashi Taniguchi, and Kenji Watanabe, and with support from the NRI-SWAN Center, Office of Naval Research, and Intel Corp.

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