Electronic Materials and Processing
Room: 210E - Session EM+MN+PS-TuA

More than Moore: Novel Approaches for Increasing Integrated Functionality
Moderator: Andy Antonelli, Nanometrics, Sean King, Intel Corporation

2:20pm **EM+MN+PS-TuA1 Maintaining the Pace of Progress as we Approach the end of Moore's Law:** ***Heterogeneous Integration, New Materials, New Processes, New Architectures***, ***Bill Bottoms***, 3MTS **INVITED**

The environment is rapidly changing as we approach the end of Moore's Law scaling. Scaling continues but benefits in performance, power and cost are reduced. At the same time drivers for the electronics industry are impacted by the emerging Internet of Things and Migration to the Cloud. Satisfying the requirements of these emerging drivers cannot be accomplished with the current technology. It will require innovative heterogeneous integration approaches to satisfy demands for power, latency, bandwidth, reliability and cost in an environment where transistors will wear out.

Overcoming the limitations of the current technology will require heterogeneous integration using different materials, different device types (logic, memory, sensors, RF, analog, etc.) and different components incorporating multiple technologies including electronics, photonics, and MEMS in new, 3D, system-in-package (SiP) architectures. New materials, manufacturing equipment and processes will be required to accomplish this and meet the market demand for continuous reduction in cost per function.

The requirements, difficult challenges and potential solutions will be discussed.

3:00pm **EM+MN+PS-TuA3 More than Moore - Wafer Scale Integration of Dissimilar Materials on a Si Platform**, ***Thomas Kazior***, *J. LaRoche*, Raytheon Company **INVITED**

Advances in silicon technology continue to revolutionize microelectronics. However, Si cannot do everything, particularly for high performance, high frequency RF and mixed signal applications. As a result circuits based on other materials systems, such as III-V semiconductors, are required. However, these other device technologies do not enjoy the integration density, cost benefit and manufacturing infrastructure of Si. So how can we get the 'best of both worlds'? What is the best way to integrate these dissimilar materials with Si? In this paper, we review different heterogeneous integration approaches and summarize our results on the successful wafer-scale, 3D heterogeneous integration (3DHI) of GaN HEMTs and Si CMOS.

Our Au-free GaN HEMTs have been successfully fabricated entirely in a Si foundry on semi-standard, 200 mm diameter Si wafers using Cu damascene interconnects. RF performance compares favorably with GaN on SiC devices fabricated in a III-V foundry with Au-based contact and interconnect metallurgy. Oxide bonding is being used to integrate these GaN on Si wafers with Si CMOS wafers. Through-dielectric-vias (TDVs) are used to interconnect the high performance GaN RF devices/circuits with high density CMOS control and logic circuits, resulting in ultra-short, wide-bandwidth interconnects enabling circuit optimization through intimate and arbitrary placement of CMOS logic and control circuitry relative to III-V devices. Through-substrate-vias (TSVs) are used for thermal management. This 'flexible' wafer-scale, integration platform is compatible with other III-V devices, other (non-Si) device/component technologies and any node of Si CMOS or SiGe BiCMOS. The 3DHI process is being used to fabricate cost effective, high performance, digitally enhanced, RF and mixed signal ICs such as 'intelligent' and adaptive/reconfigurable transceivers.

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