

# Wednesday Afternoon, October 21, 2015

## Electronic Materials and Processing

Room: 211C - Session EM+AS+MS+SS-WeA

### Surface and Interface Challenges in Wide Bandgap Materials

**Moderator:** Aubrey Hanbicki, U.S. Naval Research Laboratory, Rachael Myers-Ward, U.S. Naval Research Laboratory

2:20pm **EM+AS+MS+SS-WeA1 Effects of Nitrogen and Antimony Impurities at SiO<sub>2</sub>/SiC Interfaces**, *Patricia Mooney*, Simon Fraser University, Canada **INVITED**

4H-SiC is an attractive material for devices operating at high power and high temperatures because of the large bandgap energy, 3.23 eV, the high critical breakdown field, 2.0 MVcm<sup>-1</sup>, and high electron mobility,

850 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>. Commercialization of 4H-SiC MOSFET technology was long delayed due to the high density of defects near the SiO<sub>2</sub>/SiC interface. Post oxidation annealing in NO ambient, the process that enabled the commercialization of SiC Power ICs in 2011, significantly reduces the density of near-interface traps and results in typical effective MOSFET channel electron mobility ( $\mu_{FE}$ ) values of  $\sim 20$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> [1]. The relatively high density of near-interface traps having energy levels within 0.5 eV of the SiC conduction band was investigated using constant capacitance transient spectroscopy (CCDLTS). These measurements showed that NO annealing reduced the density of the two near-interface oxide trap distributions, attributed to Si interstitials and substitutional C pairs in SiO<sub>2</sub>, by as much as a factor of 10 [1,2].

It has also been shown that introducing impurities such as Na, P, or Sb near the SiO<sub>2</sub>/SiC interface further increases  $\mu_{FE}$ , to peak values of 104 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> and to 50 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> at high electric field for Sb [3]. The much higher value of  $\mu_{FE}$  in Sb-implanted MOSFETs was attributed to counter-doping by Sb in SiC near the interface. To investigate the effects of Sb at SiO<sub>2</sub>/SiC interfaces, Sb ions were implanted near the surface of the 4H-SiC epitaxial layer and the wafer was annealed at 1550°C in Ar to activate the Sb donors. Dry thermal oxidation was done at 1150°C and the sample was then NO-annealed at 1175°C for 30 or 120 min. CCDLTS results of Sb-implanted MOS capacitors were compared with those having no Sb implant but with similar dry oxidation and NO-annealing processes. The density of near-interface oxide traps was similar in samples with and without Sb, indicating that Sb has little effect on those defects. However, CCDLTS spectra taken at bias and filling pulse conditions that reveal defects in the SiC depletion region, show both the deeper of the two N donor levels at E<sub>C</sub> - (0.10±0.01) eV and a second energy level only in Sb-implanted samples at E<sub>C</sub> - (0.12±0.01) eV. To our knowledge this is the first measurement of Sb donors in SiC and it confirms counter doping of SiC by Sb near the SiO<sub>2</sub>/SiC interface.

[1] P.M. Mooney and A.F. Basile, in *Micro and Nano-Electronics: Emerging Device Challenges and Solutions*, Ed. T. Brozek (CRC Press, Taylor and Francis, 2014) p. 51.

[2] A.F. Basile, et al., *J. Appl. Phys.* **109**, 064514 (2011).

[3] A. Modic, et al., *IEEE Electron Device Lett.* **35**, 894 (2014).

3:00pm **EM+AS+MS+SS-WeA3 Hydrogen Desorption from 6H-SiC (0001) Surfaces**, *Sean King*, Intel Corporation, *R. Nemanich*, *R. Davis*, North Carolina State University

Due to the extreme chemical inertness of silicon carbide (SiC), *in-situ* thermal desorption is commonly utilized as a means to remove surface contamination prior to initiating critical semiconductor processing steps such as epitaxy, gate dielectric formation, and contact metallization. *In-situ* thermal desorption and silicon sublimation has also recently become a popular method for epitaxial growth of mono and few layer graphene. Accordingly, numerous thermal desorption experiments of various processed silicon carbide surfaces have been performed, but have ignored the presence of hydrogen which is ubiquitous throughout semiconductor processing. In this regard, we have performed a combined temperature programmed desorption (TPD) and x-ray photoelectron spectroscopy (XPS) investigation of the desorption of molecular hydrogen (H<sub>2</sub>) and various other oxygen, carbon, and fluorine related species from *ex-situ* aqueous hydrogen fluoride (HF) and *in-situ* thermal and remote hydrogen plasma cleaned 6H-SiC (0001) surfaces. Using XPS, we observed that temperatures on the order of 700 - 1000°C are needed to fully desorb C-H, C-O and Si-O species from these surfaces. However, using TPD, we observed H<sub>2</sub> desorption at both lower temperatures (200 - 550°C) as well as higher

temperatures (> 700°C). The low temperature H<sub>2</sub> desorption was deconvoluted into multiple desorption states that, based on similarities to H<sub>2</sub> desorption from Si (111), were attributed to silicon mono, di, and trihydride surface species as well as hydrogen trapped by sub-surface defects, steps or dopants. The higher temperature H<sub>2</sub> desorption was similarly attributed to H<sub>2</sub> evolved from surface O-H groups at  $\sim 750^\circ\text{C}$  as well as the liberation of H<sub>2</sub> during Si-O desorption at temperatures > 800°C. These results indicate that while *ex-situ* aqueous HF processed 6H-SiC (0001) surfaces annealed at < 700°C remain terminated by some surface C-O and Si-O bonding, they may still exhibit significant chemical reactivity due to the creation of surface dangling bonds resulting from H<sub>2</sub> desorption due from previously undetected silicon hydride and surface hydroxide species.

3:20pm **EM+AS+MS+SS-WeA4 Chemical and Microstructural Characterization of Interfaces between Metal Contacts and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>**, *Lisa M. Porter*, *Y. Yao*, *J.A. Rokholt*, *R.F. Davis*, Carnegie Mellon University, *G.S. Tompa*, *N.M. Sbrockey*, *T. Salagaj*, Structured Materials Industries, Inc.

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is a promising alternative to traditional wide bandgap semiconductors, as it has a wider bandgap ( $\sim 4.9$  eV) and a superior figure-of-merit for power electronics and other devices; moreover,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk single crystals have recently been grown commercially using melt-growth methods. While several groups have demonstrated Ga<sub>2</sub>O<sub>3</sub>-based devices such as Schottky diodes and MOSFETs, understanding of contacts to this material is limited. In this study, we investigated a variety of metal contacts (Ti, In, Mo, W, Ag, Au, and Sn) to both (-201)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> single crystal substrates (from Tamura Corp.) and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial layers grown by MOCVD on various substrates (sapphire and single crystal  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>) by co-authors at Structured Materials Industries. We have characterized these substrates and epilayers using techniques such as X-ray diffraction and transmission electron microscopy (TEM), which show that the epitaxial layers are oriented (-201) with respect to the substrates. We found that the electrical characteristics of the metal contacts to the Ga<sub>2</sub>O<sub>3</sub> epilayers and substrates are highly dependent on the nature of the starting surface and the resulting interface, and less dependent on the work function of the metal than expected. For example, both Ti and bulk In readily form ohmic contacts to Ga<sub>2</sub>O<sub>3</sub>, whereas other low-workfunction metals, such as Sn, did not form ohmic contacts even after annealing to 800 °C. For Ti ohmic contacts on Sn-doped Ga<sub>2</sub>O<sub>3</sub> substrates the optimal annealing temperature was  $\sim 400$  °C: the electrical characteristics continually degraded for annealing temperatures above  $\sim 500$  °C. Thermodynamics predicts that Ti will reduce Ga<sub>2</sub>O<sub>3</sub> to produce Ti oxide, therefore indicating that the Ti/Ga<sub>2</sub>O<sub>3</sub> interface is unstable. In correspondence with this prediction, high-resolution cross-sectional TEM images of 400 °C-annealed samples show the formation of an ultra-thin ( $\sim 2$  nm) interfacial amorphous layer. TEM samples at higher annealing temperature have also been prepared for analysis; electron energy loss spectroscopy will be used to characterize the interfacial composition profiles in these samples to determine the relationship between composition and thickness of the interfacial layer and the electrical degradation of the contacts. Schottky diodes with Au, Mo, W and Sn as the Schottky metal were also fabricated. The Schottky barrier heights (SBHs) showed a weak dependence on the metal workfunction. An overview of the electrical behavior of different metals as ohmic or Schottky contacts to Ga<sub>2</sub>O<sub>3</sub> and the interfacial chemistry and microstructure will be presented.

4:20pm **EM+AS+MS+SS-WeA7 Regrown InN Ohmic Contacts by Atomic Layer Epitaxy**, *Charles Eddy, Jr.*, U.S. Naval Research Laboratory, *N. Nepal*, Sotera Defense Solutions, *M.J. Tadjer*, *T.J. Anderson*, *A.D. Koehler*, *J.K. Hite*, *K.D. Hobart*, U.S. Naval Research Laboratory

For the past 25 years, compound semiconductors comprised of elements from group III-B of the periodic table and nitrogen have attracted a sustained, high-level of research focus. More recently they have found growing application to rf and power electronics in the form of advanced transistor structures such as the high electron mobility transistor (HEMT) with and without insulated gates. Key performance parameters for such devices (cut-off frequency for rf transistors and on-resistance for power transistors) are often dominated by the contact resistance. The current best approach to contact resistance minimization involves aggressive processing requirements that challenge device fabrication, especially when insulated gates are required. A potential solution is the regrowth of highly conducting semiconductor contact layers where ohmic contacts are needed.

Here we report on initial efforts to employ regrown indium nitride (InN) contact layers by atomic layer epitaxy (ALE) as a low temperature solution to the ohmic contact challenge for III-N transistors. Recently, we have reported that good crystalline quality InN can be grown at less than 250°C

by ALE [1]. Here we employ such conditions to grow very thin layers and assess them morphologically and electrically.

InN regrown contact layers of 5nm thickness grown on sapphire are very smooth (rms roughness < 0.17nm) and possess sheet resistances as low as 3.6 k $\Omega$ /sq, corresponding to electron sheet carrier densities of 2-3  $\times 10^{13}$  cm<sup>-2</sup> and mobilities of 50 cm<sup>2</sup>/V-s. These electron mobilities are higher than previously reported (30 cm<sup>2</sup>/V-s) for much thicker films (1.3  $\mu$ m) [2]. Similarly grown 22.5 nm thick InN layers on highly resistive silicon were processed with mesa isolation regions and 20/200 nm thick titanium/gold contact metals. Without any contact annealing, an ohmic contact resistance of 9.7 $\times 10^{-7}$   $\Omega$ -cm<sup>2</sup> (1.2  $\Omega$ -mm) was measured, comparable to the best high temperature alloyed contact to an AlGaIn/GaN HEMT.

In our initial non-alloyed ohmic contact process, contact regions were recessed down to the GaN buffer layer to establish physical contact between the highly-conductive InN layer and electrons in the HEMT channel. A 25 nm thick InN layer was then grown by ALE, and the InN-filled ohmic regions were then capped with a Ti/Al/Ti/Au layers. Using the metals as an etch mask, the InN outside of the ohmic regions was etched away. We will report on initial results of application of ALE InN regrown contact layers and the modified fabrication approaches to AlGaIn/GaN HEMTs.

1. N. Nepal, et al., *J Cryst. Growth and Design*, **13**, 1485-1490 (2013).
2. Kuo et al., *Diamond & Related Materials***20**, 1188 (2011).

#### 4:40pm EM+AS+MS+SS-WeA8 High-Temperature Characteristics of Ti/Al/Pt/Au Contacts to GaN at 600°C in Air, Minmin Hou, D.G. Senesky, Stanford University

The high-temperature characteristics (at 600°C) of Ti/Al/Pt/Au contacts to gallium nitride (GaN) in air are reported. GaN is a wide bandgap semiconductor material being developed for high-temperature electronics and micro-scale sensors. Ti/Al/Pt/Au metallization is frequently used for forming ohmic contacts to GaN. However, few studies have been devoted to studying the electrical characteristics of the Ti/Al/Pt/Au metallization at elevated temperatures and even fewer in oxidizing environments. It is not practical to obtain a hermetic sealing at elevated temperatures and a number of sensing applications may require non-hermetic packages. Therefore, the electrical characteristics of Ti/Al/Pt/Au contacts in a hot oxidizing ambient instead of an inert ambient or vacuum can provide new insights. In this work, the electrical and microstructural properties of Ti/Al/Pt/Au contacts to GaN upon exposure to 600°C in air are presented.

In this work, microfabricated circular-transfer-line-method (CTLM) patterns were used as the primary test structure. Ti/Al/Pt/Au were patterned through a standard lift-off process on unintentionally-doped GaN epitaxial layer grown by metal organic chemical vapor deposition (MOCVD) on sapphire. After lift-off, the samples were subject to a rapid thermal annealing (RTA) process at 850°C for 35 seconds in a nitrogen ambient.

To observe the impact of thermal exposure on the electrical and microstructural properties, the test structures were subject to a 10-hour thermal storage test in a furnace (air ambient), during which time the test structures were taken out of the furnace every two hours and their I-V characteristics were measured at room temperature. After the initial 2-hour "burn-in" period, the contact resistance remained stable over the entire remainder thermal storage test, with the variance within less than 3% and the specific contact resistivity remained on the order of 10<sup>-5</sup>  $\Omega$ -cm<sup>2</sup>.

In addition, the samples were subject to in-situ high-temperature I-V tests at 600°C in air both before and after the thermal storage using a high-temperature probe station. The linear I-V response confirms that the contacts remained ohmic after the thermal storage. The contact resistance at 600°C showed minimal change (approximately 9%) for a 20- $\mu$ m-wide gap CTLM test structure, before and after thermal storage.

The microstructural analysis with atomic force microscopy (AFM) showed minimal changes (less than 0.1%) in surface roughness after thermal storage. The results support the use of Ti/Al/Pt/Au metallization for GaN-based sensors and electronic devices that will operate within a high-temperature and oxidizing ambient.

#### 5:00pm EM+AS+MS+SS-WeA9 Schottky Contacts and Dielectrics in GaN HEMTs for Millimeter-Wavelength Power Amplifiers, Brian Downey, Naval Research Laboratory INVITED

Although GaN RF transistor technology has begun to enter commercial markets, there are still several active research efforts aimed at extending the operating frequency of GaN devices to the millimeter-wavelength (MMW) frequency range of 30 – 300 GHz. In order to facilitate power gain at MMW frequencies, both geometric device scaling and novel heterostructure/device design are required, which present interesting materials and processing challenges. In this talk, an overview of NRL's approaches to MMW GaN high-electron-mobility transistor (HEMT) technology will be presented. In one approach, N-polar GaN inverted HEMT structures are employed, which places the GaN channel at the surface of the device. In this case, Schottky

gate contacts are made directly to the N-polar GaN channel. The effect of GaN crystal polarity on Schottky barrier height will be discussed along with strategies to increase the Schottky barrier height of metals to N-polar GaN. In a second approach, Ga-polar GaN HEMTs with vertically-scaled barrier layers are utilized to reduce the surface-to-channel distance in order to maintain electrostatic control of the channel in short gate length devices. The high electric fields in these vertically-scaled barrier devices can create large tunneling-related gate leakage currents, leading to high off-state power dissipation and soft breakdown characteristics. The use of gate dielectrics in these scaled structures will be discussed including their effect on device electrical performance.

#### 5:40pm EM+AS+MS+SS-WeA11 Nitrogen as a Source of Negative Fixed Charge for Enhancement Mode Al<sub>2</sub>O<sub>3</sub>/GaN Device Operation, MuhammadAdi Negara, R. Long, D. Zhernokletov, P.C. McIntyre, Stanford University

In recent years, significant research efforts have focused on developing enhancement mode (E-mode) GaN-based devices fueled by many potential applications. Simpler power amplifier circuits using a single polarity voltage supply and increased safety using a normally-off device can be achieved using E-mode devices leading to lower cost and an improvement of system reliability. Using the combination of E-mode and depletion mode (D-mode) devices in direct coupled logic open up also new applications for nitride semiconductors. To realize normally-off operation of GaN transistors, several approaches have been reported in the past including recessed gate structures [1], p-type gate injection [2], fluorine plasma treatment [3], surface channel GaN [4], thermally oxidized gate insulator [5] and oxide charge engineering [6]. In this report, nitrogen impurities introduced during atomic layer deposition of an Al<sub>2</sub>O<sub>3</sub> gate dielectric are investigated as a means of modifying the threshold voltage ( $V_{th}$ )/flat band voltage ( $V_{fb}$ ) of GaN MOS devices. As reported in reference [7], nitrogen may incorporate on either cation or anion substitutional sites or on interstitial sites in Al<sub>2</sub>O<sub>3</sub> and become a source of negative fixed charge within Al<sub>2</sub>O<sub>3</sub>. The effectiveness of this approach for fixed charge modification of ALD-grown Al<sub>2</sub>O<sub>3</sub> compared to several alternative approaches will be presented.

References:

- [1] W. B. Lanford, et al., *Electron. Lett.* 41, no. 7, 449 (2005).
- [2] Y. Uemoto, et al., *IEEE Trans. Elect. Dev.* 54, no. 12, 3393 (2007).
- [3] Zhang et al., *Appl. Phys. Lett.* 103, 033524 (2013).
- [4] W. Huang, et al., *IEEE Elect. Dev. Lett.* 27, no. 10, 796 (2006).
- [5] K. Inoue et al., *Elect. Dev. Meet., IEDM Technical Digest. International*, pp. 25.2.1 (2001).
- [6] B. Lu, et al., in *Proc. Int. Workshop Nitride Semicond. Abstr.*,536 (2008)..
- [7] Choi et al., *Appl. Phys. Lett.* 102, 142902 (2013).

#### 6:00pm EM+AS+MS+SS-WeA12 Activation of Mg-Implanted GaN Facilitated by an Optimized Capping Structure, Jordan Greenlee, B.N. Feigelson, T.J. Anderson, K.D. Hobart, F.J. Kub, Naval Research Laboratory

For a broad range of devices, the activation of p and n-type implanted dopants in GaN is needed. The activation of implanted ions by annealing requires post-implantation damage removal and the arrangement of implanted ions in their proper lattice sites. Post-implantation activation of Mg via annealing requires high temperatures (>1300 °C). At these high annealing temperatures, GaN decomposes, leaving behind a roughened surface morphology and a defective crystalline lattice, both of which are detrimental for GaN device applications. To combat decomposition, either a high pressure environment, which is prohibitively expensive and not easily scalable, or a capping structure combined with short exposure to T >1300°C is required to preserve the GaN. In this work, we explore the effects of different capping structures and their ability to protect the GaN surface during a high temperature pulse, similar to those used in the Multicycle Rapid Thermal Annealing (MRTA) process.

It was determined that the sputtered cap provides sufficient protection for the underlying GaN during a rapid heat pulse. The in situ MOCVD-grown AlN cap, although it should have a better interface and thus provide more protection for the GaN layer, is inferior to the sputtered cap as determined by Nomarski images. After etching the surface with AZ400k developer, it was determined that the GaN underneath the MOCVD-grown cap has pits as-grown. Since both GaN layers were grown with the same recipe, we attribute these pits to the HT MOCVD AlN growth process. Atomic force microscopy was used to determine the as-grown and post annealing surface morphologies of the samples. The as-grown sample covered with MOCVD AlN does not exhibit the same smooth step flow growth as the as-grown sample without the MOCVD AlN cap. After annealing and etching off the

AlN caps, the surface that was capped with MOCVD AlN shows evidence of pitting while the sample that was protected with only sputtered AlN no longer exhibits step flow growth like the as-grown sample. Since we are above 2/3 of the melting point of GaN, we expect that bulk diffusion is occurring and causing this rearrangement at the surface. This implies that sputtered AlN can provide sufficient protection of the underlying GaN surface, which will facilitate mid-process implantation and activation of Mg in GaN.

# Authors Index

**Bold page numbers indicate the presenter**

## — A —

Anderson, T.J.: EM+AS+MS+SS-WeA12, 2;  
EM+AS+MS+SS-WeA7, 1

## — D —

Davis, R.: EM+AS+MS+SS-WeA3, 1  
Davis, R.F.: EM+AS+MS+SS-WeA4, 1  
Downey, B.: EM+AS+MS+SS-WeA9, 2

## — E —

Eddy, Jr., C.R.: EM+AS+MS+SS-WeA7, 1

## — F —

Feigelson, B.N.: EM+AS+MS+SS-WeA12, 2

## — G —

Greenlee, J.D.: EM+AS+MS+SS-WeA12, 2

## — H —

Hite, J.K.: EM+AS+MS+SS-WeA7, 1

Hobart, K.D.: EM+AS+MS+SS-WeA12, 2;  
EM+AS+MS+SS-WeA7, 1

Hou, M.: EM+AS+MS+SS-WeA8, 2

## — K —

King, S.W.: EM+AS+MS+SS-WeA3, 1  
Koehler, A.D.: EM+AS+MS+SS-WeA7, 1  
Kub, F.J.: EM+AS+MS+SS-WeA12, 2

## — L —

Long, R.: EM+AS+MS+SS-WeA11, 2

## — M —

McIntyre, P.C.: EM+AS+MS+SS-WeA11, 2  
Mooney, P.: EM+AS+MS+SS-WeA1, 1

## — N —

Negara, M.: EM+AS+MS+SS-WeA11, 2  
Nemanich, R.: EM+AS+MS+SS-WeA3, 1  
Nepal, N.: EM+AS+MS+SS-WeA7, 1

## — P —

Porter, L.M.: EM+AS+MS+SS-WeA4, 1

## — R —

Rokholt, J.A.: EM+AS+MS+SS-WeA4, 1

## — S —

Salagaj, T.: EM+AS+MS+SS-WeA4, 1  
Sbrockey, N.M.: EM+AS+MS+SS-WeA4, 1  
Senesky, D.G.: EM+AS+MS+SS-WeA8, 2

## — T —

Tadger, M.J.: EM+AS+MS+SS-WeA7, 1  
Tomba, G.S.: EM+AS+MS+SS-WeA4, 1

## — Y —

Yao, Y.: EM+AS+MS+SS-WeA4, 1

## — Z —

Zhernokletov, D.: EM+AS+MS+SS-WeA11,  
2