Plasma Science and Technology
Room: 104 C - Session PS2-TuM

Advanced FEOL/Gate Etching
Moderator: G.Y. Yeom, Sungkyunkwan University, Republic of Korea

8:00am **PS2-TuM1 Evaluation of Highly Selective ZrO_2 and HfO_2 based Hard Mask Stacks for sub 30 nm Node Dry Etch Pattern Transfer**, *J. Paul, X. Thrun, S. Riedel, M. Rudolph,* Fraunhofer Institute for Photonic Microsystems (IPMS-CNT), Germany, ***S. Wege***, Plasway, Germany, *C. Hohle*, Fraunhofer Institute for Photonic Microsystems (IPMS-CNT), Germany

The main challenge for future leading edge patterning results from an aggressive trend in reduction of resist thickness for high resolution lithography. For instance, at the 25 nm DRAM technology node, a maximum resist thickness of 30 to 60 nm is predicted by the ITRS for 2014. Moreover, the hard mask thickness will be limited by the thickness of the photoresist. Different approaches such as multi-layer resists were discussed to enable pattern transfer with reduced resist thicknesses. These approaches are focusing more and more on innovative underlayer materials and anti-reflective coatings providing a higher etch selectivity. Novel hard mask concepts with reduced layer thickness and improved etch selectivity can be seen as an alternative strategy.

The present work reveals a new hard mask concept based on ZrO_2 and HfO_2 materials in combination with a SiO_2 capping layer to provide the high resolution pattern transfer into the substrate. An excellent silicon and carbon etch selectivity is focused for semiconductor manufacturing. Besides the scaling capability, the hard mask concept was evaluated in terms of etch selectivity, hard mask roughness, removal of remaining hard mask after etch and cost-saving deposition method. Therefore atomic layer and spin-on depositions of HfO_2 and ZrO_2-based hard masks were investigated. Additionally the influence of dopants on the etch properties and patterning results was evaluated.

The dual hard mask concept was demonstrated using 35 nm thin layers of ZrO_2 and HfO_2 based material and 45 nm SiO_2 deposited on 300 mm wafers. The resist (50 nm) was directly applied on the hard mask and arrays of holes and trenches (CD 30 nm to 500 nm) were printed by electron beam direct writing. The hard mask open was performed in a two-step process by CCP and ICP type etch chambers. The hole and trench pattern were transferred into silicon and carbon by dual-frequency MERIE CCP and triple-frequency CCP type etch system, respectively. Finally the remaining mask was removed by wet etching without deterioration of the etched profiles. This sequence allowed the preparation of structures with aspect ratios up to 20:1 (CD 30 to 60 nm) and revealed a high overall hard mask selectivity to silicon e.g. ~ 35:1.

This new dual-layer concept enables a significant reduction of overall hard mask thickness and the patterning of 30 nm structures and a potential technology approach for more critical structures in the sub 20 nm range.

8:20am **PS2-TuM2 Approach to LER/LWR Improvement with Combination of DCS Technology and Newly Developed Resist Material**, ***M. Honda***, *K. Kobayashi,* Tokyo Electron Miyagi Limited, Japan, *M. Yamato, K. Oyama, H. Yaegashi, H. Mochiki*, Tokyo Electron Limited, Japan

Due to the continued scaling in semiconductor industry, reducing line edge roughness (LER) and line width roughness (LWR) during photoresist mask pattern transfer by etch becomes increasingly important at 10nm and beyond.

Our previous studies showed that successful LER/LWR reduction was achieved by optimizing plasma treatment conditions and DC superposition (DCS) technology which is resist hardening by highly energetic electrons incident onto wafer in DC+RF hybrid capacitively-coupled reactor [1,2]. On the other hand, newly developed PMMA-based 193nm resist material with low etching durability has been proposed for the further reduction of LER/LWR [3,4].

In this paper, we investigated the effect and mechanism of DCS technology on newly developed 193nm resist material. As a result, we achieved LER=1.2nm with new 193nm resist material by etching durability enhancement of DCS technology. We also found that DCS technology is very effective for CD shrink control especially required for future BEOL patterning. This integrated solution of resist material modification and DCS technology will allow us for expanded process window for LER/LWR control at 10nm and beyond critical patterning etch.

Reference

[1] M. Honda et al., Proc. of SPIE 8328-09 (2012)

[2] M. Honda et al., AVS 59th Int. Symp. & Exhibit. (2012)

[3] H.Yaegashi et,al,. Proc. of SPIE 8325-11 (2012)

[4] K.Ohmori et, al., Proc. of SPIE 8325-12 (2012)

8:40am **PS2-TuM3 Metrology and Linewidth Roughness Issues during Complex High-k/Metal Gate Stack Patterning for sub-20nm Technological Nodes**, ***E. Pargon***, *M. Fouchier,* CNRS-LTM, France, *O. Ros Bengoechea,* STMicroelectronics, *J. Jussot,* UJF, France, *E. Dupuy, M. Brihoum*, CNRS-LTM, France **INVITED**

Gate Line Width Roughness (LWR) or Line Edge Roughness (LER) is considered today as a factor limiting CMOS downscaling. No technological solution is currently known to reach the 1.7nm gate LWR required for the sub-20nm technological node. The origin of the LWR/LER of the final transistor gate is mainly attributed to the significant roughness of the photoresist (PR) pattern printed by the lithography step, which is partially transferred into the gate stack during the subsequent plasma etching steps. Thus, those passed few years, many efforts have been focused on the development of post-lithography resist treatments in order to minimize the LWR of resist patterns prior to plasma transfer. Another issue related to LWR/LER is the availability of accurate and convenient metrology tools for their evaluation. The status on LER/LWR metrology is that there is today no reliable and efficient metrology equipment to determine LWR at the very bottom of structures, where the key LWR information lies, as well as to estimate sidewall roughness of complex high-k/metal gate stacks composed of a multitude of very thin layers of dielectrics, metals and semiconductors.

We first propose a method based on AFM to measure LER accurately down to feature bottom for any types of pattern profiles (anisotropic, tapered or re-entrant). We will show that it presents a great potential for better understanding the mechanism of LER transfer during complex high-k/metal gate stack patterning.

Various post-lithography processes based on thermal or plasma treatments are also evaluated to decrease resist pattern LWR. A particular attention is paid to characterize the roughness by its frequency spectrum since for gate applications low frequency roughness components remain the key issue. We will show that optimized plasma treatment for LWR reduction may use plasma conditions leading to intense optical emission in the vacuum ultra violet (VUV) range (<200nm), and limiting the deposition of carbon outgassed resist byproducts on the pattern sidewalls. Moreover, we show that thermal process applied after plasma treatment can improve further the resist LWR, provided that no carbon deposition be previously formed on the resist sidewalls during the plasma treatment. The best available post-lithography treatment allows a 50% LWR reduction, while maintaining the critical dimension control. Finally, the developed AFM technique is used in comparison with CD-SEM to study the transfer of the reduced resist LWR resist into the gate stack during the patterning.

9:20am **PS2-TuM5 Possible Si Damage Formation and Redeposition in Vertical Gate Etching Processes by HBr Plasmas**, ***Y. Muraki***, *H. Li, T. Ito, K. Karahashi,* Osaka University, Japan, *M. Matsukuma,* Tokyo Electron Ltd., Japan, *S. Hamaguchi*, Osaka University, Japan

Reactive ion etching (RIE) by halogen-based plasmas such HBr plasmas are widely used for Si etching in semiconductor manufacturing processes. It has been know that, for a Si surface, Br ions have high etching yields, high selectivity over SiO2 and SiN, and high etching anisotropy. However, in recent years, as non-classical CMOS structures such as vertical multi gates have been introduced for near-future devices, there has been a concern on possible damages caused by highly energetic hydrogen ions (H+) that hit a Si surface even at grazing angles. For vertical multi gates, the Si surfaces subject to direct ion bombardment function as gate channels, ion bombardment damage to the surface must be minimized. In this study, we have evaluated sputtering yields of Si by Br+, H+ and SiBr+, as functions of incident energy in the range from 300 eV to 1000eV as well as functions of the incident angle. We have also examined Si substrate damages caused by ion bombardment by transmission electron microscopy (TEM) and High-resolution Rutherford Backscattering Spectrometry (HRBS). It has been found that there is strong angle dependence of the Si etching yield by Br+ ion irradiation, which indicates that Br+ ion etching has also an aspect of physical sputtering despite its high chemical reactivity with Si. Although, in actual HBr plasma processing, simultaneous surface passivation by Br radicals makes its Si etching more chemical, the nature of physical sputtering by energetic Br+ ion bombardment ensures anisotropic etching. The depth of damages in a Si substrate caused by Br+ ion bombardment, on the other hand, decreases with its angle of incidence as Br+ ions cannot

penetrate deeply into the substrate at higher incident angles. However, it has been also found that energetic H+ ions can be damaging to the Si surface even at large incident angles since, due to their small mass, incident H+ ions are scattered nearly isotropically when they hit the substrate surface. In addition, due to their small atomic size, H+ ions penetrate far more deeply than Br + ions do. Furthermore it has been found that SiBrx+ ions can be deposited at low energy. Since, at relatively high-pressure, SiBrx+ ions can be rather abundant in HBr plasmas for Si etching. Therefore care must be taken in developing HBr etching processes for vertical multi gates to avoid surface damages by H+ ions and to control the profiles despite incident and/or re-sputtered species with higher sticking probabilities.

9:40am **PS2-TuM6 Impact of Etch Processes Over Dimensional Control and LWR for 14nm FDSOI Transistor Gate Patterning***,* ***O. Ros***, ST Microelectronics, France

Microelectronic evolution still relies on higher transistor gate integration and transistor size reduction. The major issue related to transistor downscaling is the control at the nanometer range of two main variability sources: Critical Dimension uniformity (CDU) and the Line Width Roughness (LWR). Nowadays, the best lithography conditions allow the definition of photo-resist patterns with a minimum roughness of 4-5nm and a CDU at 3σ < 2.5nm (for 28nm technologies), which will be then transferred into the underlying layers by etch processes. To improve lithography performances, post-lithography treatments such as plasma treatments have so far been introduced to increase photo-resist stability and to improve LWR and CDU during pattern transfer. If such a strategy allows to meet the CDU and LWR requirements of the 32 nm technological node, we will show that the unique use of conventional post-lithography treatments is not anymore efficient to address the specifications of the latest CMOS and beyond CMOS technologies. They indeed introduce several pattern deformations such as resist flowing and gate shifting, that inevitably cause process variability. Thus, new patterning strategies have to be implemented to ensure CMOS downscaling.

In this study, we compare different etch chemistry combinations in order to define the best etch process condition to pattern a 14 nm Fully Depleted Silicon On Insulator (FDSOI) gate stack guaranteeing control over the main variability sources, CD uniformity and LWR. We show that a combination of photo-resist pre-treatments and an optimization of each material's etch process are required to ensure process control during typical FDSOI gate stack patterning (consisting in Photoresist/Silicium Anti Reflective Coating (SiARC)/Carbon layer (SoC)/Oxide Hard Mask (HM)/Polysilicium/High-K Metal Gate (HKMG)). As an example, promising results over SiARC opening step show that the introduction of a new etch chemistry followed by an optimized trim step leads to better defined patterns and a 25% improvement over LWR compared to the values obtained after standard SiARC opening.

10:40am **PS2-TuM9 FinFET Patterning: Promises and Challenges of SIT^2 for Fin Formation for sub-40 nm Pitch Features***, S. Mignot,* GLOBALFOUNDRIES U.S. Inc.*, I.C. Estrada-Raygoza, H. He,* IBM*, K. Akarvardar, J. Cantone,* GLOBALFOUNDRIES U.S. Inc.*, B. Doris,* IBM*, A. Jacob,* GLOBALFOUNDRIES U.S. Inc.*, S. Schmitz, J. Lee,* ***P. Friddle****, M. Goss*, Lam Research Corp

FinFET device enables scaling of CMOS technology due to its reduced short-channel effects. Realization of this potential is highly dependent on achieving ideal fin structure shape and reducing variability at the front-end of the process. In particular, fin width and high uniformity are critical. The width of the fin structure is typically required to be at a critical dimension that is below resolution limit of single exposure conventional 193nm immersion lithography (i.e, <40nm half pitch). Over the last couple of technology nodes one common technique for fin formation at tight pitch is to use patterning process flow of Sidewall Image Transfer (SIT).

In this publication, a Double Sidewall Image Transfer (SIT^2) etch patterning process has been demonstrated for sub 40nm pitch at fin step. The SIT^2 process scheme that has been explored includes silicon mandrel etch followed by Nitride Spacer deposition and etch. Process integration at this level requires a process free of collapsing features and with minimum pitch variations. SIT^2 main etch challenges will be reviewed. Etch process mechanisms both physical and chemical have been investigated to achieve silicon etch fin pattern and selectivity to the hard mask and spacer materials as well as uniformity for both macro-to-macro and across wafer.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

11:20am **PS2-TuM11 Stack Patterning Challenges for the FinFET Architecture***, A. Banik,* ***S. Kanakasabapathy****, S. Burns, A. Aiyar, M.J. Brodsky*, IBM Corporation

The FinFET device architecture, presents certain new gate patterning challenges. The gate stack aspect ratio is higher, compared to previous planar generations. We will illustrate how this aspect ratio is due to the presence of fins and the need for higher overetch in the offset spacer patterning. Controlling the gate profile to be vertical in both isolated and dense lines is challenging as the gate height increases. Further, Double expose Double etch (DE^2) has been the process of record since the 45nm node. This is driven by the need for better tip-to-tip control while maintaining across chip line width control (ACLV). It has typically relied on pattern assembly through DE^2, in the gate hardmask layers, followed by a transfer etch into the underlying gate polysilicon. In such a scheme, the dense-iso gate critical dimension (CD) variation is exacerbated by the tall gates needed for the FinFET architecture. Legacy techniques, such as higher ion energy in the polysilicon etch, are limited by the large overetch needed past the fin tops, and selectivity needed in that step.

We present in this paper, patterning sequencing options that reduce the dense-iso challenges for the unique FinFET geometry. We will present data that shows how Lithography and etch process modifications are needed to enable such modified patterning sequences.

This work has been performed by the independent SOI technology development projects at the IBM Microelectronics Division Semiconductor Research & Development Center, Hopewell Junction, NY 12533

11:40am **PS2-TuM12 Mechanisms of Etching and Selectivity for FINFET Gate Low-k Spacer using RLSA™ Microwave Plasma Reactor with Radial Line Slot Antenna***,* ***A. Raley****, B. Parkinson, A. Ranjan, S. Keisuke, K. Kumar, P. Biolsi*, TEL Technology Center, America, LLC

Spacer design and materials for planar and FINFET transistors has becomes increasingly critical as gate length is shrinking. For technology node of 22nm and beyond, fringe capacitance between gate and contact/epi-facet are becoming significant component of device degradation.[1] Spacer films with low dielectric constant (Low-k spacer) minimize parasitic capacitances because low permittivity can reduce gate-fringing field effects. Several materials and methods for low-k spacers have been reported showing improved device performance[2,3]. Incorporation of oxygen, boron, and carbon into SiN spacer film to form SiOCN or SiBCN low-k films with oxygen, boron and carbon contents tuned to minimize k value and provide good leakage performance are two of the low-k avenues being explored. Etching of these materials versus conventional SiN spacer has been characterized in simulated wafer product environment and demonstrated on FINFET structure using RLSA™ microwave plasma reactor with radial line slot antenna. RLSA™ microwave plasma source yields high ion flux with tunable ion energies to control polymer passivation. This is key to achieve the high SiN/Si and SiN/SiO2 selectivities mandated by long over etch requirement in the FINFET spacer scheme. The etching mechanisms of low-k films have been compared to that of SiN and SiO2 and it has been shown to strongly depend on the oxygen content of the film. A systematic study on process parameters impact on low-k film etching rate versus SiN and SiO2 will be presented. Optical emission spectra analysis of relative intensities of the following species F, B, H, CF2, and O will be analyzed. Impact of electron energy distribution (tuned by source power and pressure) and ion angular energy distribution (tuned by bias power and pressure) on the species considered will be shown to explain selectivity mechanisms and etch rate trends.

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2. Ko, C.H, "A novel CVD-SiBCN Low-k spacer technology for high-speed applications", VLSI Technology Symposium, 2008, p108-109

3. Huang, E., "Low-k spacers for advanced low power CMOS devices with reduced parasitic capacitances", SOI Conference, 2008. SOI. IEEE International, p10-20

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