Plasma Science and Technology
Room: 104 C - Session PS-MoA

Advanced BEOL/Interconnect Etching

Moderator: S. Hamaguchi, Osaka University, Japan

2:00pm **PS-MoA1 Etching Challenges in the BEOL for sub 20nm Technology Nodes**, ***K. Kumar***, *Y.P. Feurprier, L. Wang, J. Stillahn, Y. Chiba, A. Ranjan, A. Metz, A. Ko, D.M. Morvay, A. Selino, P. Biolsi*, TEL Technology Center, America, LLC **INVITED**

In the sub-32nm technology node, Trench First Metal Hard Mask (TFMHM) integration scheme has gained traction and become the preferred integration of low-k materials for BEOL. This integration scheme also enables Self-Aligned Via (SAV) patterning which prevents via CD growth and confines via by line trenches to better control via to line spacing. In addition to this, lack of scaling of 193nm Lithography and non-availability of EUV based lithography beyond concept, has placed focus on novel multiple patterning schemes. This added complexity has resulted in multiple etch schemes to enable technology scaling below 80nm Pitches, as shown by the memory manufacturers. Double-Patterning and Quad-Patterning have become increasingly used techniques to achieve 64nm, 56nm and 45nm Pitch technologies in Back-end-of-the-line. Challenges associated in the plasma etching of these integration schemes, along with the challenges posed with etching EUV resists, in concert with shape formation of the dual-damascene will be discussed in the presentation.

2:40pm **PS-MoA3 Plasma Etch Challenges at 10nm and beyond Technology Nodes using Multi Patterning Techniques in the BEOL to Produce Metallization-Friendly Profiles**, *Y. Mignot*, STMicroelectronics, *M. Beard, B.G. Morris, B. Peethala*, IBM, *Y. Loquet*, STMicroelectronics, *J.H. Chen*, IBM, *S. Nam*, GLOBALFOUNDRIES U.S. Inc., *B. Nagabhirava*, ***P. Friddle***, Lam Research Corp

As feature critical dimension (CD) shrinks towards and beyond the 48nm pitch, new patterning techniques within the context of a trench-first-metal-hard-mask (TFMHM) patterning scheme have been developed to generate trenches and vias below 48nm pitch. One of the main challenges at advanced nodes is to create structures (i.e., trenches & vias) that can be robustly metalized. This requires several elements of focus for the etches: first, there must be zero dielectric etch damage that results in undercut of any hard masks in the film stack; second, the aspect ratio of the final etch structure must be minimized; and third, the shape of the trench or via profile must be tailored to be metallization-friendly (i.e., slight angle better than vertical) and finally a good selectivity on lower metallization in case of wet HMO faceting. These requirements often conflict with each other, especially within a patterning scheme that requires self-aligned vias, where the desired high selectivity to the hard mask conflicts with the need to minimize the amount of hard mask left in order to decrease aspect ratio. In this paper, we will discuss some of the approaches that we have investigated to achieve the best profile for metallization. This includes plasma etch all-in-one (AIO) dielectric etch optimization as well as multi-step solutions that potentially can use techniques including wet chemistries plus dry faceting and dry metal HMO removal. In addition, data will present on overview of the multi-patterning techniques such as multiple Litho-Etch (LE3), Sidewall Image transfer (SIT) and double patterning for self aligned via (DPSAV) to expose and understand the multiple underlying interactions at Dielectric RIE such as the SIT Block Mask with the DPSAV features.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities

3:40pm **PS-MoA6 Fine Patterning of Copper by Plasma Etch Process for Advanced BEOL Interconnects**, ***H. Miyazoe***, IBM T.J. Watson Research Center, *M. Hoinkis*, Applied Materials Inc., *B.N. To, G. Fritz, A. Pyzyna, M. Brink, C. Cabral*, IBM T.J. Watson Research Center, *C. Yan, I. Ne'eman*, Applied Materials Inc., *E.A. Joseph*, IBM T.J. Watson Research Center

As device scaling continues beyond the 10 nm node, challenges in back end of line (BEOL) interconnect technology continue to multiply. Expanding beyond the known issues of patterning and integration of porous ultra low-k (ULK) materials, new issues such as line edge roughness and line width roughness (LER/LWR) as well as increased resistivity (emanating from grain boundary scattering) are only compounding the difficulties at hand and may require significant modifications to the typical damascene integration flow. Subtractive etching of Cu has a potential to overcome current difficulties in interconnects integration such as the increase of resistivity caused by electron scattering at grain boundary, poor coverage of liner/seed materials, and a time dependent dielectric breakthrough (TDDB) issue of ULK material by starting from blanket Cu film with large crystal (>1 μ m), by depositing it directly on Cu patterns, and by minimizing plasma damage during ULK etch, respectively. In this work, we examine one such alternative approach to conventional dual damascene copper integration, in which subtractive patterning of copper is employed. Successful patterning of copper at smaller than 50 nm critical dimension (CD) with smaller than 100nm in pitch is demonstrated using a novel high density plasma based dry etch process. Consisting of a reactive sputter based etch chemistry, appreciable etch rates on the order of ~15A/s are achieved, with high selectivity (>6:1) to masking layers. The angle of sidewall of approximately 85° was achieved at an optimized condition while we obtained ~45° in case of physical sputtering using pure Ar plasma. We confirmed that the resistivity of fabricate Cu line increases with the decrease of line CD. The resistivity of isolated Cu line at CD of ~30 nm is ranging from 10 to 20 μohm cm. A full review of the etch process, its mechanism and the positive implications on ULK materials, LER and LWR, metal resistivity and overall reliability will be discussed in detail.

4:00pm **PS-MoA7 Virtual Fabrication for BEOL Module Optimization Beyond the 22nm Technology Node**, ***R. Patz***, *D. Fried, K. Greiner, M. Stock, D. Faken, J. Lehto, A. Pap, B. van Dyk, M. Kamon, S. Breit*, Coventor, Inc.

Virtual fabrication provides a powerful platform for exploring process interactions in 3D, reducing time-consuming and costly trial-and-error silicon experimentation. A Trench First Metal Hard Mask BEoL integration scheme including Self-Aligned Vias (TFMHM-SAV) has been characterized using a M1-V1-M2 example. Experiments focused on the patterning operations involved, and were based on 64nm Mx pitch designs. Variation studies were used to determine the key drivers of V1-M1 contact area, liner coverage and via spacing. A full-wafer study showed the impact of patterning and deposition non-uniformity. This full-wafer virtual fabrication data can focus attention on the most critical unit processes and enable Automated Process Control (APC).

V1-M1 contact area, a critical electrical and reliability criterion, was primarily determined in this integration scheme by M1 lithography bias. Through a +/- 3nm range of M1 exposure, the contact area varied more than 3x, from 322nm^2 to 1091nm^2. Chamfer profile, critical for electromigration reliability, was dictated by the Mx Overetch (OE) depth and sputter ratio (ion energy). Cross-sectional analysis was used to characterize the final metallization, enabling conclusions regarding resistance and yield. TiN selectivity during the M2 etch dominated the profile, leading to metallization differences. Surprisingly, the cross-sectional area of Mx copper decreased slightly (~3%) with reduced TiN selectivity (from 40:1 to 10:1), a change that opened the top profile and was expected to lead to improved copper fill. 3D model inspection revealed that this effect was driven by a "shoulder" in the cap layer, resulting in a metallization profile degrade.

Geometries beyond the 22nm technology node and resulting unit process requirements push the limits of process tool capability and cross-wafer uniformity. A module-level approach must be considered to compensate for uniformity limitations of any single process by adjusting specifications elsewhere in the process flow. A full-wafer virtual fabrication experiment explored cross-wafer deposition and patterning variation in the M1-V1-M2 module to quantify the aggregate effect of many realistic unit process steps on the fully-integrated structure. While these cross-wafer variations yielded a 1sigma uniformity of 12% in Mx copper cross-sectional area, the sensitivities lay the foundation for APC-based yield improvement.

4:20pm **PS-MoA8 Improvements in Low-k Damage and Hard Mask Selectivity in BEOL Dielectric Etch Using C5HF7**, ***R.L. Bruce***, IBM T.J. Watson Research Center, *T. Suzuki, M. Nakamura*, Zeon Chemicals LP, *S.U. Engelmann, E.A. Joseph, N. Fuller, E.M. Sikorski*, IBM T.J. Watson Research Center, *A. Itou*, Zeon Corporation

As feature sizes continue to decrease, significant issues are found using highly selective fluorocarbon gases to etch interconnect low-k dielectrics. Three examples of these challenges include; line wiggling, low-k damage, and low selectivity (e.g. to organic masks). To address these challenging issues, we have evaluated C5HF7 and other novel etch gases for 14nm and 22nm devices to determine if they enable the optimized fabrication of BEOL interconnects. Etch performance is assessed for both trench and via patterns and also when incorporated into full dual-damascene structures. Compared to conventional fluorocarbon etch gases such as C4F6 and CF4/CHF3 mixtures, experiments with C5HF7 have shown a substantial increase in low-k dielectric to metal hard mask and capping layer selectivity for trench and self-aligned via etching. Low-k damage is also investigated by post-etch HF treatment to measure critical dimension loss from

dissolution of plasma-damaged dielectric. A significant reduction in damage is observed with C5HF7 in low-k films of two different dielectric constants. Finally, we propose a mechanism for high selectivity, low damage dielectric etch at sub-80nm pitch structures using rationally-designed novel etch gases.

4:40pm **PS-MoA9 Mitigation of Plasma-induced Damage of Advanced 2.0 Porous Dielectrics by the Pore Stuffing Approach**, ***M.H. Heyne***, *L. Zhang*, KU Leuven, Belgium, *J.-F. De Marneffe, R. Gronheid, C.J. Wilson, M. Baklanov*, IMEC, Belgium

Plasma-induced damage is a major hurdle for the integration of 2.0 dielectrics in advanced interconnects targeting sub-10 nm nodes. State-of-the-art low-k dielectrics are porous organo-silicate glass (p-OSG) films, with high carbon content and interconnected porosities up to 50 %, making the material sensitive to modifications by plasma reactive radicals and VUV photons. A possible solution is the so-called pore stuffing approach: after porogen burnout, a sacrificial polymer is introduced into the porous matrix, hampering diffusion of radicals in the bulk material and attenuating VUV light propagation.

PECVD ultra-low-k dielectric films with k = 2.0 and porosity of 40 – 50 % were stuffed with PMMA. The protection efficiency was evaluated against fluorocarbon-based, oxygen-based plasmas and 147 nm VUV light generated in industrially relevant 300 mm CCP chambers. The material damage was determined by FTIR, spectroscopic ellipsometry, ellipsometric porosimetry, TOF-SIMS, water contact angle measurements, and capacitance measurements. Plasma damage was significantly reduced in PMMA protected samples, resulting in lower hydrophilicity, smaller carbon loss, smaller fluorine penetration, and lower dielectric constants in comparison to unprotected material. PMMAs of molecular weights between 2000 and 7000 g/mol influenced the filling conditions and filling process window, but gave similar level of plasma protection. Plasma-induced VUV light led to significant PMMA degradation, through carbonyl bonds depletion and formation of other polymer by-products, resulting in only a short-term protection of the dielectric against 147 nm radiation. Pattern transfer for 40 nm lines required small changes in discharge parameters, and resulted in lowered sidewall damage when compared to non-stuffed samples.

After the etching, the polymer is usually removed from the pores by a thermal burn-out above 400°C, which is not compatible with BEOL processing. An alternative approach is proposed, using a non-damaging He/H_2 downstream plasma at 280°C, allowing a full CMOS process compatibility.

Pore stuffing is a promising approach to mitigate the plasma damage in porous ultra-low-k material by using a temporary hybrid material approach. In contrast to former hybrid solutions, this one is not suffering from shrinkage or material interaction and therefore, might allow one further step to $k_{eff} \leq 2.0$ interconnect systems.

5:00pm **PS-MoA10 EPR Studies of SiOC:H BEOL (Low-k) Dielectrics**, ***T.A. Pomorski***, *P.M. Lenahan, M. Mutch,* Penn State University, *S.W. King*, Intel Corporation

Low-κ interlayer dielectrics with dielectric constants significantly less then those of SiO_2 and are utilized to reduce capacitance induced RC delays in ULSI circuits. [1,2] At the present time, very little is known about the underlying physical mechanisms involved in electronic transport within these films. Recent electron paramagnetic resonance (EPR) studies have reported on defect centers in some of these films [3,4]. In one study, comparisons were made between EPR defect densities and leakage currents before and after exposure to UV light under conditions generally similar to those during industrial UV curing. That study noted that large UV induced changes in spin density were accompanied by large changes in dielectric leakage, suggesting a link between the defects and leakage.[3] In this study we have conducted a considerable more extensive survey specifically focused upon low-k SiOC:H films. We find that a large variety of paramagnetic centers are present in the dielectrics and that both the types of defects present and the defect densities are quite strong functions of processing parameters. Defects include silicon dangling bond centers in which the silicon is back bonded to three oxygens (E" centers), silicon dangling bond centers complexed to a single hydrogen atom, a dangling bond center complexed to three equivalent hydrogens, and very likely carbon dangling bond centers. In, limited cross section of samples, all with the EPR dominated by a center with a zero crossing g=2.0026 +/- 0.0003 and all similarly processed, we observe strong correlation between defect density and dielectric leakage currents. It should be noted that quite recent SiOC:H studies which have utilized another analytical approach has also identified the presence of E' centers in similar films. King et. al. recently reported on reflection electron energy loss spectrometry (REELS) on similar dielectric films and noted the presence of REELS spectra consistent with E' centers a result which our EPR data supports.[5]

[1] K. Maex, D. Shamiryan, F. Iacopi, S.H. Brongersma, and Z.S. Yanovitskaya, J. Appl. Phys, **93**, 11 (2003).

[2] W. Volksen, R.D. Miller, and G. Dubois, Chem Rev. **110**, 56 (2010).

[3] B. Bittel, P. Lenahan, S. King, Appl. Phys. Lett. **97**, 6 (2010)

[4] H. Ren, et. al. Appl. Phys. Lett. **98**, 10 (2011)

[5] S.W. King, B. French, E. Mays, J. Appl. Phys, 113, 044109 (2013)

5:20pm **PS-MoA11 Effect of NH_3/N_2 Ratio in Plasma Treatment on Porous Low Dielectric Constant SiCOH Dielectric**, ***Y.L. Cheng***, *J.F. Huang, T.C. Bo*, National Chi-Nan University, Taiwan, Republic of China

The influence of N_2/NH_3 ratio in the plasma treatment on physical, electrical properties and reliability characteristics is investigated in this study. It is found that all the plasma treatments resulted in the formation of a thin and modified layer on the surface of the porous low-*k* films, and the properties of this modified layer is affected by N_2/NH_3 ratio in the plasma. Results indicate that pure N_2 plasma treatment forms an amide-like layer on the surface, which apparently leads to a higher increase in the dielectric constant. A mixture of N_2/NH_3 gas plasma treatment induces more moisture uptake on the low-*k* dielectric's surface, which degrade the electrical performance and reliability. Among N_2/NH_3 gas plasma treatment, plasma-treated low-*k* dielectric has better electrical and reliability characteristics as N_2/NH_3 gas ratio equals to 1.

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