Manufacturing Science and Technology
Room: 202 B - Session MS+AS+EM+NS+PS+TF-MoA

IPF 2013-Manufacturing Challenges for Emerging Technologies: III. Manufacturing Challenges: Electronics

Moderator: D. Seiler, National Institute of Standards and Technology (NIST), J. Hollenhorst, Agilent Technologies

2:00pm **MS+AS+EM+NS+PS+TF-MoA1 Graphene Materials and Devices Roadmap**, ***L. Colombo***, Texas Instruments **INVITED**

The advancement of graphene and graphene based products will require a research and development progression similar to materials and development programs are now in full production, e.g. Si industry. The graphene research community has made significant progress over the past nearly a decade now in the physics and chemistry of graphene. We are now full engaged in the materials and device development and in some cases initial product stages. The introduction of any graphene based product will require the identification of materials, device and product metrics in order to properly keep track of the progress toward the product goals. In this presentation I will review and discuss the roadmap for various graphene based applications and present the status of materials and devices for nanoelectronic applications.

2:40pm **MS+AS+EM+NS+PS+TF-MoA3 Devices and Materials for the Post CMOS Area - What Are We Looking For?**, ***W. Haensch***, IBM T.J. Watson Research Center **INVITED**

The long predicted end of scaling is coming. Many times it was predicted that the IC industry will hit a brick wall. Beginning in the early 1980's when pattering solutions were doomed to fail, then through the late 1990's when gate oxide scaling was thought to be at its end, and now in the recent years when device performance is thought to hit its physical limits. The truth is however that none of these posed an obstacle that could not be addressed. The reason while the progress of the industry enjoyed in the last several decades is slowing down is related to the ever increased power consumed to achieve ever higher performance. Seeing the end approaching, the quest for what is coming next is on! In this presentation I will give short review how we got where we are and what are the wonderful properties of MOSFET devices that allowed this extraordinary development. I will then look at the possibilities of a possible extension of the existing core logic technology. Finally I will discuss some alternate device options and provide a critical evaluation how they might fit into the IT landscape.

3:40pm **MS+AS+EM+NS+PS+TF-MoA6 Manufacturing Challenges of Directed Self-Assembly**, ***R. Gronheid***, IMEC, Belgium, *P.A. Rincon Delgadillo,* University of Chicago, *T.R. Younkin,* Intel Corporation, *B.T. Chan, L. Van Look, I. Pollentier,* IMEC, Belgium, *P.F. Nealey*, University of Chicago **INVITED**

Directed Self-Assembly (DSA) of block copolymers (BCP) is based on nano-scale phase separation. Depending on the relative volume fraction of the blocks, different morphological structures may form in the bulk of these materials. In the case of di-block copolymers, specifically the lamellar and cylindrical phase provide structures that may be used to form line/space and hole-type patterns, respectively. When thin films of BCPs are applied on substrates that provide a pre-pattern to guide the assembly process, the orientation and direction of the resulting structures can be controlled. DSA has gained significant attention as a next method for mainstream nano-fabrication in a time span of just a few years. The primary interest in the DSA technology includes the inherent variability control (since dimension is controlled through the polymer molecular weight) and the high pattern densities (typical length scales are on the order of 3-50nm) that are accessible. The outstanding questions that need to be answered in order to prove readiness of DSA for semiconductor manufacturing include defectivity, pattern transfer capabilities, pattern placement accuracy, design rule restrictions that are imposed by DSA and demonstration in an electrically functional device.

At imec, DSA based patterning has been implemented on 300mm wafers in various process flows that are compatible with semi-conductor manufacturing. These flows have been used as test vehicles to study the above-mentioned issues. In this paper, an overview will be given of the main recent accomplishments from the imec DSA program.

4:20pm **MS+AS+EM+NS+PS+TF-MoA8 Phase Change Memory**, ***R. Bez***, Micron, Italy **INVITED**

Phase Change Memory (PCM) is a Non-Volatile Memory (NVM) technology that provides a set of features interesting for new applications, combining features of NVM and DRAM. PCM is at the same time a sustaining and a disruptive technology. From application point of view, PCM can be exploited by all the memory systems, especially the ones resulting from the convergence of consumer, computer and communication electronics. PCM technology relies on the ability of chalcogenide alloys, typically $Ge_2Sb_2Te_5$ (GST), to reversibly switch from amorphous state to poly-crystalline state. The two stable states differs for electrical resistivity, thus the information is stored in the resistance of the bit.

The alteration of the bit is possible thanks to melt-quench of the active material achieved by fast (10-100ns) electrical pulses. The energy delivered to program a bit is in the order of 10pJ, with a state of the art access time of 85ns, read throughput 266MB/s and write throughput 9MB/s. These peculiar features combined with data retention, single bit alterability, execution in place and good cycling performance enables traditional NVM utilizations but also already opened applications in LPDDR filed. Moreover PCM is considered the essential ingredient to push to the market the so called Storage-Class Memory (SCM), a non-volatile solid-state memory technology that is capable of fill the gap between CPU and disks.

In this perspective PCM technology can be effectively exploited in wireless systems, in solid state storage subsystem, in PCIe-attached storage arrays and in computing platform, exploiting the non-volatility to reduce the power consumption.

In order to be able to enter into a well established memory market there are key factors that must be fulfilled: i) match the cost of the existing technology in terms of cell size and process complexity, ii) find application opportunities optimizing the overall "memory system" and iii) provide a good perspective in terms of scalability. Phase Change Memory has been able so far to progress in line with all these requirements. Aim of this presentation is to review the PCM technology status and to discuss specific opportunities for PCM to enter in the broad memory market.

5:00pm **MS+AS+EM+NS+PS+TF-MoA10 450 mm Project**, ***P. Farrar***, University at Albany-SUNY **INVITED**

The talk will focus on the leadership role the G450C consortium in driving the industry transition from 300mm to 450mm wafers. The current Status of the work at CNSE will be explored as well as the key role this public private partnership play is developing the process capability Required for High Volume Manufacturing. In addition critical success factors, and the ability to manage in a collaborative manner will be focused on.

Authors Index

Bold page numbers indicate the presenter

— B —

Bez, R.: MS+AS+EM+NS+PS+TF-MoA8, **1**

— C —

Chan, B.T.: MS+AS+EM+NS+PS+TF-MoA6, 1
Colombo, L.: MS+AS+EM+NS+PS+TF-MoA1, **1**

— F —

Farrar, P.: MS+AS+EM+NS+PS+TF-MoA10, **1**

— G —

Gronheid, R.: MS+AS+EM+NS+PS+TF-MoA6, **1**

— H —

Haensch, W.: MS+AS+EM+NS+PS+TF-MoA3, **1**

— N —

Nealey, P.F.: MS+AS+EM+NS+PS+TF-MoA6, 1

— P —

Pollentier, I.: MS+AS+EM+NS+PS+TF-MoA6, 1

— R —

Rincon Delgadillo, P.A.: MS+AS+EM+NS+PS+TF-MoA6, 1

— V —

Van Look, L.: MS+AS+EM+NS+PS+TF-MoA6, 1

— Y —

Younkin, T.R.: MS+AS+EM+NS+PS+TF-MoA6, 1