Tuesday Afternoon, October 29, 2013

Manufacturing Science and Technology Room: 202 B - Session MS+AS+EL+EM+PS+TF-TuA

Manufacturing Challenges of Nanoscale Patterning

Moderator: E.B. Svedberg, The National Academies

2:00pm MS+AS+EL+EM+PS+TF-TuA1 Alphabet-Based Template Design Rules - A Key Enabler for a Manufacturable DSA Technology, H. Yi, H-.S.P. Wong, Stanford University INVITED

Block copolymer DSA is a result of spontaneous microphase separation of block copolymer films, forming periodic microdomains including cylinders, spheres, and lamellae. Among all the various self-assembled structures, cylinder patterns have attracted specific interest due to their great potential in patterning electrical contacts in Integrated Circuits (ICs). Due to the random distribution of electrical contacts in layouts as well as the continuous scaling of IC circuits, patterning contacts has become increasingly challenging for traditional optical lithography. Due to the advantage of low cost and sub-20 nm feature sizes, block copolymer directed self-assembly (DSA) is a promising candidate for next generation device fabrication.

Traditionally, the study of DSA has been focused on achieving long range order and a periodic pattern in large area. Chemoepitaxy approaches including using chemical patterns of preferential affinity on the substrate surface or controlling pattern formations by tuning annealing conditions have been investigated and developed. They can improve the long range order self-assembly quality and lower the defect density over large areas. In order to use DSA to pattern the randomly distributed contacts in IC layouts, we adopt physical (topographical) templates to form irregularly distributed cylindrical patterns. Topographical templates use strong physical confinements in lateral directions to alter the natural symmetry of block copolymer and guide the formation of DSA patterns. Previously we have demonstrated that for the first time the self-assembled features can be almost arbitrarily placed as required by circuit fabrication and not limited to regular patterns, by combining templates of different types on one wafer. These various templates are akin to the letters of an alphabet and these letters can be composed to form the desired contact hole patterns for circuit layouts. The capability of arbitrary placement is demonstrated in industryrelevant circuits such as static-random-access-memory (SRAM) cells and standard logic gate libraries at a dimension that is the state-of-the-art semiconductor technology today [1]. To enable introduction of DSA into manufacturing we developed a general template design strategy that relates the DSA material properties to the target technology node requirements. This design strategy is experimentally demonstrated for DSA contact hole patterning for half adders at the 14 nm and 10 nm nodes [2]. Reference:

[1] H. Yi et al. Adv. Mater, 2012.

[2] H. Yi et al. SPIE, 2013.

2:40pm MS+AS+EL+EM+PS+TF-TuA3 Characterizing the Sensitivity of Block Copolymer Directed Self-Assembly Processes to Material and Process Variations, C. Henderson, A. Peters, R. Lawson, P. Ludovice, Georgia Institute of Technology

Future scaling of integrated circuits (IC) is in jeopardy due to a number of challenges related to both future material and process requirements that are needed to allow for fabrication of sub-20 nm IC devices. One of the most critical challenges is that of developing patterning technologies that can allow for formation of sub-20 nm patterned structures in a fast and economically viable manner. Due to difficulties with alternative technologies, techniques that can extend the use of current 193 nm optical lithography in a cost effective manner would be very attractive. Directed Self-Assembly (DSA) using block copolymers to perform pitch subdivision of lithographically generated primary patterns is one such promising technology. In this technique, a lithographic method is first used to define a topographic or chemical template pattern on a surface. This surface is then coated with a block copolymer that is further processes to induce microphase separation. The presence of the topographic or chemical patterns on the surface aligns, registers, and provides long range order to the formed block copolymer patterns. This microphase separation-based patterning process utilizes the propensity of the block copolymer to naturally form nanometer scale patterns whose size are dictated by the polymer block molecular weight.

The overarching goal of our work has been to develop both new block copolymers that can enable sub-20nm DSA patterning and to develop the experimental and modeling tools needed to understand the limits of such

processes. In this paper, we will review our recent systematic studies of block copolymer DSA processes using state-of-the-art molecular dynamics simulations. The aim of these studies has been to identify the important material and process factors that affect the DSA process and to quantify the sensitivity of the DSA process to these factors. For example, the influence of polymer block molecular weight control and polydispersity on patterning have been rigorously quantified. Furthermore, processing factors such as guiding pattern mis-sizing and low level surface topography in the guiding pattern and their effect on DSA patterning have been studied in detail. Studies have also been performed via simulation using thermodynamic integration methods to calculate the free energy of defects in such DSA systems and the sensitivity of such defect free energies to important material and process parameters. We will review the outcomes of these studies to illustrate what the important material and process challenges will be in adapting block copolymer DSA methods into a manufacturable technology.

3:00pm MS+AS+EL+EM+PS+TF-TuA4 DSA Patterning for sub-40 nm Pitch Features, *I.C. Estrada-Raygoza, C. Liu, Y. Yin, J. Abdallah,* IBM Albany Nanotech Center, *S. Mignot,* GLOBALFOUNDRIES U.S. Inc., *B.G. Morris, M.E. Colburn,* IBM Albany Nanotech Center, *V. Rastogi, N. Mohanti, A. Raley, A. Ko,* TEL Technology Center, America, LLC

As the semiconductor industry targets sub-40 nm pitch features, there will be a necessity for new patterning techniques which allow for the extension beyond single ArF-immersion patterning capability of 38 half pitch features. To meet today's aggressive design requirements, double patterning techniques, such as Pitch Splitting (PS) Lithography and Sidewall Image Transfer (SIT), have been widely used. Below 38 nm pitch design the industry has looked toward Extreme Ultraviolet (EUV), Double Sidewall Image Transfer (SIT2) and Directed Self-Assembly (DSA) as strong emerging candidates. A major component to the success of the DSA technique is the development of effective etch processes. This talk targets to discuss the challenges and innovations of the plasma etch process on sub-40 nm pitch features produced by DSA chemo and grapho-epitaxy guiding patterns. Each DSA scheme presents different challenges, depending of the aspect ratio, density of the patterns and etch stack materials, but in general, the parameters that have been studied are selectivity to both masking and etched materials, across wafer profile uniformity, critical dimension (CD) uniformity and line-edge/line-width roughness (LER/LWR). This work was performed by the Research Alliance Teams at Albany IBM Research and Development Facilities.

4:40pm MS+AS+EL+EM+PS+TF-TuA9 Advanced Gate Patterning Techniques for 14nm Node and Beyond, F.L. Lie, R. Jung, Y. Yin, A. Banik, S. Kanakasabapathy, J.C. Arnold, S. Seo, B. Haran, IBM Corporation, Y. Moon, L. Jang, S. Bentley, GLOBALFOUNDRIES U.S. Inc., H. Kang, D. Bae, Samsung Electronics Co., A. Metz, C. Cole, K. Ito, S. Voronin, A. Ko, A. Ranjan, K. Kumar, TEL Technology Center, America, LLC

For advanced CMOS nodes, traditional patterning processes are challenged to meet the technology needs of certain key levels. For example, conventional 193nm immersion lithography is not able to resolve features below 40nm half pitch with a single exposure without severe design rule restrictions. Until further wavelength scaling through Extreme Ultraviolet (EUV) has matured, the industry's attention is focused on advanced patterning schemes such as Pitch Splitting (PS) Lithography and Sidewall Image Transfer (SIT). In PS, a pattern is defined by two lithography exposure with a certain coordinate shift between the two exposures. PS can be achieved through either litho-etch-litho-etch or litho-litho-etch. In SIT, a pattern is defined by creating a mandrel in one lithography exposure, depositing a conformal spacer film on the mandrel, and pulling out the mandrel, resulting in two standing spacer for the pattern frequency doubling. This work evaluated the advantages and technical challenges of PS and SIT patterning schemes for line-space application. We will focus on CD uniformity improvement, line edge/line width roughness control, pitch walk control, and the extendability of each technique. RIE challenges common to double patterning such as through pitch etch bias will also be discussed

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities and in joint development with TEL Technology Center, America, LLC

5:00pm MS+AS+EL+EM+PS+TF-TuA10 High Throughput Electrospinning of Ceramic Nanofibers, S. Sood, P. Gouma, State University of New York at Stony Brook (Stony Brook University)

High yield nanomanufacturing has been the focus of greater attention due to the emerging importance of functional nanomaterials. Electrospinning is a

nanomanufacturing process that faces challenges as far as its scalability is concerned. Even the existing high-throughput electrospinning systems are limited to processing thin layers of polymer nanofibrous mats. Nanofibrous ceramics have rarely been studied with respect to their electrospinning processing. On the other hand, electrospun nanowires of ceramics are key to nanotechnology and nanomedicine applications (e.g. electrospun MoO₃ nanowires have been used as ammonia sensors for application in noninvasive diagnostics [1]). In this study, the scalable synthesis of ceramic oxide nanomats by the multi-jet design that we developed and built and which enables very high yield of ceramic nanofibers is discussed. As a scaled up approach to traditional needle electrospinning [2], up to 24 jets are spun simultaneously using similar processing parameters as a traditional needle set up. Due to a thin metallic disc design, with tiny holes drilled at the disc, the electric field is evenly distributed to all jets. Continuous replenishment of the source disk at higher flow rates allows for high yields of nanofibers.

P. Gouma, K. Kalyanasundaram, and A. Bishop, "Electrospun Single Crystal MoO3 Nanowires for Bio-Chem sensing probes", Journal of Materials Research, Nanowires and Nanotubes special issue, 21(11), pp. 2904-2910, 2006.

S. Sood, S. Divya, P. Gouma, "High throughput electrospinning of 3D nano fibrous mats". Journal of Nanoengineering and Nanomanufacturing. Accepted Publication. In Print, 2013.

5:20pm MS+AS+EL+EM+PS+TF-TuA11 Manufacture and Characterization of Silver and Copper Nanorods Produced via Forcespun Nylon 6 Nanofibers Templates, D.M. Mihut, K. Lozano, W. Zhao, The University of Texas Pan American

The Nylon 6 nanofibers are produced using the forcespinning method and further on coated with metallic thin films using the thermal evaporation equipment. The Nylon 6 nanofibers are used as templates in order to obtain silver and copper nanorods where the polymer is removed after high temperature calcination from the metallic coated structures. The metallic nanorods morphology and electrical behavior are characterized using the scanning electron microscopy, scanning transmission electron microscopy (SEM, STEM), energy dispersive X-ray spectroscopy (EDX) and electrical measurements. This method of fabrication offers the ability to obtain controlled ultrafine size netallic nanorods.

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