Electronic Materials and Processing
Room: 101 B - Session EM1-WeM

Electrical Testing and Defects in III-V's
Moderator: C.L. Hinkle, University of Texas at Dallas

8:20am **EM1-WeM2 Formation and Properties of High-k/InGaAs Interfaces on Well-Controlled Surfaces**, ***P.C. McIntyre***, Stanford University **INVITED**

Electrically active defects that either trap carriers or act as centers of fixed charge are critically important in MOS devices. Their effects are particularly pronounced for arsenide-based semiconductors intended for NMOS devices because of 1) the relative ease of forming surface defects on these crystals, 2) the lack of an insulating native oxide (such a SiO_2) to inhibit tunneling of electrons from the substrate into near-interface defects in deposited gate dielectrics, and 3) the low density of states in the conduction band of the semiconductor that enhances the effect of charge traps on the measured capacitance compared to materials such as Si or Ge. Alloying GaAs with InAs reduces the band gap of the former by lowering the energy of the conduction band edge, reducing the overall density of defect states in the band gap and thus the density of interface traps. Further reduction in both bulk dielectric defect densities (e.g. border traps and fixed charge) and interface trap densities can be achieved by appropriate pre-dielectric and post-dielectric processes. This presentation will review recent results on pre-atomic layer deposition defect passivation, including trimethyl aluminum and oxidant pre-dosing of initially clean and oxide-free InGaAs (100) surfaces, plasma treatments of initially air-exposed surfaces, and post-dielectric defect passivation using hydrogen. Reliable interface trap density measurements that combine capacitance-voltage and conductance-voltage analysis indicate trends in interface trap density across the band gap (down to ~ 10^{12} $cm^{-2}eV^{-1}$ near midgap) and in border trap density as a function of the different passivation treatments. Results obtained from MOS capacitors fabricated on As_2-decapped InGaAs (100) substrates are compared with reported density functional theory predictions and scanning probe measurements of InGaAs surface defect passivation.

9:00am **EM1-WeM4 Chemical Passivation of GaAs using Alkanethiols**, ***P. Mancheno-Posso***, *A.J. Muscat*, University of Arizona

III-V semiconductors are among the most promising materials for low-power and high-speed electronic devices owing to their high electron mobility and high breakdown fields. For instance, their use as channel materials would enable an increase in performance without changing the transistor density. Despite these advantages, III-V materials lack a defect-free and stable native oxide that could be used as a dielectric in metal-oxide-semiconductor field-effect transistors (MOSFET). Moreover, the most widely studied III-V semiconductor, GaAs, contains interfacial oxides that detrimentally affect its electronic performance. Etching the oxides and depositing a passivation layer that hinders oxidation is one approach to incorporate III-V materials in high volume production. Chemical passivation layers containing S have shown particular promise and were deposited using the precursors Na_2S, $(NH_4)_2S$, and alkanethiols. The alkyl chain on the thiols can act as a diffusion barrier to prevent oxygen from reaching the III-V surface, if the thiol molecules can be closely packed. In this study, alkanethiols with chain lengths from 3-20 carbon atoms were deposited from the liquid phase on GaAs (100), and their effectiveness in preventing oxidation in ambient conditions was characterized using ellipsometry, X-ray photoelectron spectroscopy (XPS), and Fourier-transform infrared spectroscopy (FTIR). The C 1s XPS peak showed that thiols with longer carbon chains exhibited higher surface coverages, as well as reduced surface oxidation after ambient exposure. FTIR peaks at 2918±1 and 2850±1 cm^{-1}, corresponding to asymmetric and symmetric stretches of CH_2 moieties, demonstrated the formation of a well ordered monolayer for chains with 18 and 20 carbon atoms. In addition, XPS and temperature programmed desorption confirmed the successful desorption of the carbon chains of thiols after annealing in vacuum to 750 K. Atomic layer deposition (ALD) of Al_2O_3 using a TMA and water process showed that film nucleation and growth was reduced by a factor of about two on the thiol-passivated surface compared to the liquid-cleaned surface. Although the initial film growth was slowed, a thiol passivation layer could broaden the use of III-V semiconductors in device manufacturing.

9:20am **EM1-WeM5 Disorder Induced Gap States in III-V MOS Devices**, ***E.M. Vogel***, Georgia Institute of Technology **INVITED**

Frequency dispersion is a commonly observed feature in the experimental capacitance-voltage characteristics of III-V MOS devices. This characteristic has been reported on a wide variety of III-V substrates in conjunction with many different dielectrics. The conventional interface state capacitance model, which works extremely well for Si devices, does not accurately model the frequency dispersion observed in III-V systems. Different models have been developed to explain the origin of this frequency dispersion. One model, disorder induced gap states (DIGS), attributes this dispersion to the tunneling of carriers into a disordered region caused by oxidation of the III-V substrate which is close to the interface between the III-V substrate and an insulator. A separate model attributes this dispersion to border traps located inside and associated with the high-k dielectric. In this talk, electrical characterization, modeling and physical characterization is used to demonstrate that the observed frequency dispersion must be due to the disruption of the crystalline III-V semiconductor during oxide deposition and not due to border traps located in the high-k dielectric.

10:40am **EM1-WeM9 III-V Frequency Dispersion in CV and Small Signal AC Transconductance Measurements**, ***H.C. Lin***, IMEC, Belgium **INVITED**

High-Mobility n-MOSFET option with InGaAs channels are of intense interests. As the well-known interfacial trap (D_{it}) problem appears now contained, new challenges are emerging from above the interface. The evidence of oxide border traps (BT) in high-k dielectrics and its effect on the on-state performance of InGaAs n-MOSFETs are presented in this study through combined CV dispersion and AC transconductance analyses. Frequency dispersion in CV measurements can be associated with conductive losses of the MOS system. At different gate bias the conductive loss due to events such as minority carrier generation-recombination, trapping/de-trapping at the dielectric/III-V interface and within the dielectrics can be observed. By carefully examine the multi-frequency CV and GV response we can establish the conductance spectroscopy of the MOS device. Frequency dispersion in strong accumulation can be the result of oxide trapping. By measuring the device at different temperatures we have observed strong temperature dependence in CV dispersion at accumulation. The AC transconductance (AC-gm) measurement resembles the conventional CV measurement except for the additional small drain bias applied to inject carriers across the channel. This small but crucial difference allows one to examine the effect of oxide border traps on carrier transport. Clear frequency dispersion is observed on both the CV and AC-gm response of the InGaAs MOSFET. The increase in AC frequency reduces both the trapping time constant and the charging of the border traps, resulting in lower capacitance and yet higher peak transconductance. The amount of frequency dispersion on the AC-gm curves reflects the border trap density close to the oxide-semiconductor interface and clearly shows the impact of the traps on carrier transport.

11:20am **EM1-WeM11 High-k Dielectric/InGaAs MOSCAPs with EOTs 0.7 nm and Low Interface Trap Densities**, ***V. Chobpattana***, *S. Stemmer*, University of California, Santa Barbara

A major challenge for future high performance metal-oxide-semiconductor field effect transistors (MOSFETs) is the development of high-k dielectrics, such as Al_2O_3 and HfO_2. A large density of interface traps (Dit) is typical for highly scaled dielectrics on III-V semiconductor channels and causes inefficient Fermi level response or even Fermi level pinning. In this presentation, we show a novel surface preparation method using alternating cycles of nitrogen plasma and trimethyaluminum (TMA) pulse on III-V surface before atomic layer deposition (ALD) of HfO_2 gate stack. We show that nitrogen plasma cleaned stacks exhibit much reduced frequency dispersion in depletion that is due to midgap D_{it} even for highly scaled stacks. This technique allows for highly scaled HfO_2/n-$In_{0.53}Ga_{0.47}As$ gate stacks with equivalent oxide thicknesses (EOTs) of less than 0.7 nm and midgap D_{it} values less than $4x10^{12}$ cm^{-2} eV^{-1}. Interface trap densities are characterized by capacitance-based and conductance methods. High-quality HfO_2 MOSCAPs exhibit accumulation capacitance densities above 2.5 $\mu F/cm^2$. We report on the interfacial layer thickness, analyze the interface chemistry and bonding, and discuss the reason for the improve performance of nitrogen plasma cleaned gate stacks.

11:40am **EM1-WeM12 Effect of Deposition Temperature on the Electrical Properties of ALD-HfO_2 Film on GaAs**, ***S. Choi***, *Y.-C. Byun, Y. An, H. Kim*, Sungkyunkwan University, Republic of Korea

For the scaling of n-channel metal-oxide-semiconductor field-effect transistor (NMOSFET) down to a sub-10 nm-node, atomic layer deposition (ALD) of high-*k* gate dielectrics on III-V channel materials has been widely studied to achieve excellent dielectric quality comparable to that on Si. Nevertheless, there are still many remaining issues to be solved and the most important one is a poor interface quality. The high interface state

density is believed to be closely associated with the existence of substrate element-related oxide bonds near the interface region [1]. In this presentation, we systematically investigated the electrical properties of ALD-HfO_2 films on both n-type and p-type GaAs substrates as a function of the ALD temperature and compared with those on Si substrates. Based on several physical and chemical probing methods, we tried to understand the identity of near-interface characteristics and to correlate with the resulting electrical properties. For the initial surface preparation before the ALD process, n- and p-type GaAs substrates were cleaned with HF and S-passivated using $(NH_4)_2S$ solution. For the HfO_2 deposition, tetrakis (ethylmethylamino) hafnium/H_2O precursors were used, and the ALD temperature was varied from 200 °C to 300 °C. According to the high frequency capacitance-voltage measurement, the frequency dispersion in the accumulation region was somewhat decreased when the deposition temperature was lowered. The interface trap density (D_{it}) distribution across the GaAs bandgap was estimated based on the conductance measurements conducted on both n- and p-type GaAs samples. This also exhibited a decreasing trend with decreasing ALD temperature. Detailed discussion on various physical/chemical analysis results such as X-ray photoelectron spectroscopy and time of flight-secondary ion mass spectrometry will be presented and compared with the similar experimental results performed on the Si substrates.

[1] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, *Appl. Phys. Lett.*, **86**, 152904 (2005).

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