Electronic Materials and Processing
Room: 101 B - Session EM-WeA

III-V Devices and Tunnel FETs

Moderator: P.C. McIntyre, Stanford University, E.M. Vogel, Georgia Institute of Technology

2:40pm **EM-WeA3 Plasma Enhanced ALD of High-k Dielectrics on GaN and AlGaN: Interface Formation, Growth, and Electronic States**, ***R.J. Nemanich***, *B.S. Eller, J. Yang*, Arizona State University **INVITED**

The disparate polarization at AlGaN/GaN heterostructures engenders a 2D electron gas (2DEG) that effectively reduces on-resistance and power loss, resulting in a high electron mobility ideal for high-frequency, high-temperature, and high-voltage requirements associated with HFETs and HEMTs. Since GaN and AlGaN are characterized by a large spontaneous polarization, there is a large polarization bound surface charge ($2.2x10^{13}$ and $3.2x10^{13}$ charges/cm^2) that must be compensated presumably by states near the dielectric-GaN or dielectric-AlGaN interface. While specific failure mechanisms have yet to be identified, it is clear that these states may play a role in gate leakage and current collapse. Recent efforts to improve performance of high power devices have focused on the role of a high-*k* dielectric as a gate oxide between the gate metal and AlGaN/GaN and as a surface passivation layer between the gate and source-drain contacts. The use of a specific dielectric requires a large band gap and band offsets that confine carriers in the semiconducting layers. Moreover, the concentration of the 2DEG is directly affected by the presence of interface states and defect states associated with the dielectric. In this research, we have employed remote plasma enhanced ALD (PEALD) and *in-situ* photoemission spectroscopy to prepare and characterize different dielectric layers on GaN and AlGaN surfaces. The *in-situ* x-ray and UV photoemission (XPS and UPS) measurements provide insight into the interface bonding, presence of impurities, band alignment, and band bending, which indicate the presence of defects. This report will concentrate on the properties of PEALD Al_2O_3 and HfO_2 layers on AlGaN and GaN on both the Ga-face and N-face. Results establish that the band alignment is relatively independent of processing and may be described by the charge neutrality level model. In contrast, the band bending is dependent on processing and can be directly related to the presence of charged defect states at the interface and in the dielectric. The wet chemical and *in-situ* surface cleaning processes and the PEALD growth affect the band bending, resulting in similar band bending regardless of the surface polarization. This consistency indicates the presence of interface states that compensate the polarization charge on Ga- and N-face surfaces even though the polarization charge is opposite in sign and for GaN and AlGaN surface where the polarization charge increases by a factor of two. The interplay of polarization and the defect states and the 2DEG properties are discussed for the different dielectric layers and processing approaches.

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4:00pm **EM-WeA7 Graphene-based Vertical Heterostructures and Tunneling Field Effect Transistors**, *K. Lee, K. Kim, B. Fallahazad, S. Larentis, M.S. Points,* ***E. Tutuc***, The University of Texas at Austin **INVITED**

We discuss the realization of vertical heterostructures consisting of two-dimensional materials, such as graphene and transition metal dichalcogenides, using a layer-by-layer transfer approach. We demonstrate double layer heterostructures consisting of two graphene layers separated by a thin hexagonal boron nitride dielectric, with layer mobilities as high as 200,000 cm^2/Vs. We discuss the in-plane electron transport as a function of temperature and in magnetic fields, as well as the tunneling between the two layers, which can be used as basis for vertical field-effect transistors.

4:40pm **EM-WeA9 Quantum Mechanical Corrections for Accurate and Rapid Analysis of III-V/High-k MOS Devices**, *R. Galatage,* ***C.L. Hinkle***, University of Texas at Dallas, *E.M. Vogel*, Georgia Institute of Technology

The measurement, modeling, and extraction of MOS relevant parameters from high-k on III-V semiconductors is significantly more challenging than that for Si gate stacks. Oxidation of the III-V material during high-k deposition leads to an extremely high interface trap density (D_{it}) as well as tunneling of carriers into defects further away from the interface. Additionally, the exact band structure of III-V semiconductors is a matter of ongoing research,[1] and the effects of band non-parabolicity and quantization have not been thoroughly investigated. Each of these considerations is crucial in the proper analysis of III-V MOS devices.

Due to the high electric fields, quantum mechanical effects have a significant impact on the electrical properties of scaled MOS devices. In accumulation and inversion, quantization results in the splitting of the once continuous energy bands into discrete subbands and moves the charge centroid away from the semiconductor/dielectric interface. Both of these effects reduce the inversion and accumulation charge density at a given gate bias resulting in both a threshold and flatband voltage shift, as well as a reduction in the inversion and accumulation capacitances. Therefore, it is imperative that quantum mechanical effects be considered to accurately extract the EOT, V_{fb}, and D_{it} when researching these devices. Full Schrodinger/Poisson solvers are available to calculate the carrier concentration in a physically accurate and self-consistent manner. However, these calculations take considerable computation time and cannot be used to extract parameters from an experimental data set.

In this work, we implement quantum mechanical corrections to *rapidly extract* relevant III-V MOS C-V parameters by approximating the quantization effects as an effective increase in the semiconductor bandgap in accumulation and inversion in a manner similar to that of van Dort for Si.[2,3] When coupled with non-parabolic energy bands, these approximations are shown to be quite accurate in modeling and extracting the characteristics of III-V/high-k devices. These approximations have been rigorously tested against experimental III-V devices as well as benchmarked with full Schrodinger/Poisson solutions to ensure their accuracy. This implementation allows for the rapid assessment of III-V parameters .

This work is sponsored by the SRC Global Research Corporation.

1 T. P. O'Regan, et al., *Applied Physics Letter,* 96,103705, 2010.

2 M. J. Van Dort, *Solid-State Electronics*, 37, 411, 1994.

3 E. M. Vogel, et al., *Solid State Electronics,* 47, 1589, 2003.

5:00pm **EM-WeA10 The Physics and Challenges of Realizing High Performance Group IV Tunnel Transistors**, ***J.C.S. Woo***, *H.-Y. Chang, B. Adams, P.-Y. Chien, J. Li*, University of California at Los Angeles**INVITED**

Reducing the standby power ($I_{OFF}* V_{DD}$) and operation power ($C_gV_{DD}^2*f$) are crucial for low power application in MOSFET scaling. Hence, it becomes essential to lower I_{OFF} and to scale V_{DD}, and therefore devices with steep subthreshold swing (SS) are highly desired in low power application [1].

In conventional MOSFETs, the subthreshold swing is limited by thermal diffusion current (≥ 60mV/dec at T=300K). To overcome this limit, novel devices based on the band-to-band tunneling mechanism, namely tunnel FET (TFET), is proposed. It has been reported that TFETs can achieve ultra-high I_{ON}/I_{OFF} under reduced V_{DD} and steep SS (<60mV/dec), which makes it a competitive candidate for low power application [2-3]. However, reported results so far show that TFET can only provide small I_{ON} and achieve steep SS under low current level. These short comes may prevent TFET from entering main stream.

To resolve these challenges, it is important to understand the physics of TFET. Based on these insights, small band-gap materials such as SiGe and Ge have been proposed to improve carrier tunneling by lowering the tunnel barriers [4-5]. It is also critical to improve carrier tunneling (that is, reducing the tunneling distance) by enhancing lateral electric field across the tunneling junction. TFETs with dopant pocket between source and channel are reported as one of the devices to achieve small tunneling distance [6]. In this talk, n-i-p Si TFET with p^+ pocket source fabricated by laser annealing is proposed and investigated. By the application of source pocket in TFET, the tunneling distance is reduced due to enhanced electric field across the tunneling junction. The steep SS (46mV/dec), excellent I_{ON}/I_{OFF} ratio (>10^7) and improved output characteristics are observed in the experiment data at T=300K. The device performance of this TFET under low temperature measurement is also used to confirm the band-to-band tunneling mechanism. Finally, compared to other TEFTs, the TFET with source pocket is one of the most promising structures to improve the device characteristics of TFETs.

[1] R. Jhaveri et al., *Trans. Elec. Dev.*, vol. 58, no. 1, pp. 80-86, 2011.

[2] F. Mayer et al., *IEDM Tech. Dig.*, 2008, pp. 163–166.

[3] K. Jeon et al., *VLSI Symp. Tech. Dig.*, 2010, pp. 121–122.

[4] D. Kazazis et al., *Appl. Phys. Lett.*, vol. 94, no. 26, pp. 263508-1 – 263508-3, 2009.

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