Electronic Materials and Processing
Room: 102 A - Session EM-ThA

Materials and Process for Advanced Interconnects II

Moderator: S.W. King, Intel Corporation, E. Mays, Intel Corporation

2:00pm **EM-ThA1 Electrically Detected Magnetic Resonance of Deep Level Centers in SiCN:H Dielectrics**, ***M. Mutch***, *P.M. Lenahan,* Penn State University, *S.W. King*, Intel Corporation

SiCN:H films have great promise as etch stop layers in interlayer dielectric structures [1]. Unfortunately, very little is known about the physical mechanisms of electronic transport in these materials. In this study we have utilized variable field electrically detected magnetic resonance (EDMR) almost certainly via spin-dependent trap-assisted tunneling (SDT) in variable range hopping [2]. Our results of are of significance for several reasons. First, they demonstrate that SDT/EDMR is sensitive enough to detect defects involved in transport within these films. The simple observation of an EDMR spectrum undoubtedly links the defects responsible for the spectrum to electronic transport. Secondly, they provide information about the physical and chemical nature of the defects involved of transport within the films.

The films studied were deposited via PECVD and have a composition of 45% Si, 29% C, 23% N and 3% O. The SDT/EDMR measurements were taken on a home-built X-band (≈9.5 GHz) EDMR spectrometer at room temperature utilizing specially thinned SiCN:H films deposited on p-type silicon with titanium electrode. We observe quite strong SDT/EDMR traces with a zero crossing of g = 2.003 and a peak-to-peak line width of 14 Gauss. (The g is determined by the expression $g = h\nu/(\mu_B B)$, where h is Planck's constant, ν is microwave frequency, $\mu_B$is the Bohr magneton and B is the magnetic field at resonance. We find that the SDT/EDMR response is quite strongly voltage dependent and find a fractional contribution of the SDT/EDMR response to be highly asymmetric, with a much larger ΔI/I corresponding to negative gate polarity. It is clear that the paramagnetic sites observed to not involve electron wave function primarily localized on either hydrogen or nitrogen as both of these nuclei have virtually 100% abundant isotopes with nuclear moments [3]. The zero crossing of g = 2.003 and a 14 G line width are essentially a perfect match with the well characterized EPR spectrum of K-centers, silicons back-bonded to three hydrogens. The K-centers have been studied extensively in silicon nitride [4, 5]. We thus tentatively assign the observed EDMR to K-centers and also tentatively conclude that the K-centers are important defects in transport in SiCN:H films under study.

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[5] P. M. Lenahan et. al, Appl. Surf. Sci. 39, 392 (1989).

2:20pm **EM-ThA2 Effect of Hybrid Cleaning in Mitigating Low-k Damage for Critical BEOL Applications at 20 nm Node and Beyond**, ***N. Mohanty***, *J. Stillahn, Y.P. Feurprier, T. Yoshida, T. yamamura, L. Wang, Y. Chiba, K. Kumar, D.M. Morvay, P. Biolsi,* TEL Technology Center, America, LLC, *S. Mishra, W. Hwang, M. Wang*, GLOBALFOUNDRIES U.S. Inc.

Integration of low-k dielectrics (k ≤ 2.7) into the fabrication of interconnects in integrated circuits has enabled the reduction of RC time delays, opening the path for continued scaling. Typical porous low-k dielectrics are formed by plasma-enhanced chemical vapor deposition and contain a significant amount of Si-CHx groups. For the ubiquitous trench-first metal hard mask dual damascene scheme, etching of the via holes into the low-k dielectric is mostly achieved using a fluorocarbon chemistry, after which a cleaning step is needed for concomitant in-situ removal of etch residues as well as the top organic mask for subsequent underlying trench pattern transfer. The cleaning step can either be reductive (N2, H2 containing feed gas) or oxidative (O2, CO2, CO containing feed gas). Owing to their higher reactivity, mild oxidative chemistries comprised of CO2 feed gas have been the predominant chemistry of choice industry-wide, which minimizes the depletion of –CHx groups known as low-k damage while maintaining reasonable etch rates. However, as the industry moves on to advanced technology nodes (sub 20 nm nodes), even minor damage during the cleaning step becomes highly undesirable due to increased RC delay and diminished reliability. This talk will present the successful mitigation of low-k damage as compared to standard cleaning processes through the use of a novel two-step hybrid cleaning strategy. This two-step hybrid cleaning strategy leverages unique hardware solutions with the reactive ion etching efforts for reducing low-k damage.

2:40pm **EM-ThA3 Cu Interconnects at 1x Node - Challenges & Approaches**, *S. Kesapragada,* ***K. Shah***, Applied Materials, Inc. **INVITED**

While much attention is focused on transistor innovation, it is interconnect performance that is

also now challenging Moore's law because of its performance and scaling limitations. The last

time interconnects were overhauled for performance reasons was more than 15 years ago when

aluminum was replaced with copper interconnects fabricated in the revolutionary dualdamascene

architecture.

Copper dual-damascene interconnects provided superior lower resistance, and the incorporation

of porous low-k dielectrics into this architecture drove down the capacitance – together these two

materials have reduced RC delay and reduced energy consumption. However, the reduction of

the low-k dielectric constant has slowed in recent years. As they become more porous, these

dielectric materials become fragile, unable to cope with the mechanical stress that chips undergo

during packaging. They are not robust enough to maintain their low-k properties through the

dual-damascene process integration steps. In addition, the resistance of the interconnect is rising

dramatically because of three main factors: (i) the conventional tantalum nitride/tantalum highresistance

metallic barriers that block copper diffusion and prevent oxidation are taking up a

larger fraction of the metal interconnect cross-section, (ii) surface scattering increases as the

critical dimensions of the wires become smaller than the bulk mean free path of the electrons,

and (iii) grain boundary scattering increases as the copper grain size scales approximately with

the critical dimensions of the wires in dual-damascene fabricated interconnects. Hence, the RC

delay for interconnects has started to rise dramatically as the node shrinks beyond 22nm, driven

by the rise in resistivity for conventional damascene copper interconnects. This presentation

looks at process and integration-level inflections that promise to limit RC delay increase while

also achieving void-free gap fill in nano-scale interconnects.

3:40pm **EM-ThA6 Selective Deposition of Cu Film in Recessed Features using a Hollow Cathode Magnetron Physical Vapor Deposition Source**, ***A. Dulkin***, *I. Karim, H. Qiu, E. Ko, R. Tarafdar, K. Colinjivadi, J. Hahn, K. Leeser, K. Ashtiani*, Lam Research Corp

Copper filled vias and trenches in dielectrics are the building blocks of the dual damascene interconnect metallization in VLSI. The fill is traditionally done with electroplating, which is preceded by physical vapor deposition (PVD) of a Cu seed layer. PVD film is known to have poor conformality within a recessed structure, with the top of the feature sidewall getting thicker coverage than the bottom. The resulting film coverage profile is not favorable for subsequent plating. Advances in iPVD technology have improved conformality; however, as the size of the features decreased below 40nm, achieving conformal seed coverage became increasingly undesirable. Conformal deposition increases the effective aspect ratio (AR) of the features, thereby making the subsequent electrofill process more challenging. Hence, bottom-up film growth which forms a seed profile with a thick bottom and continuous but not too thick sidewall coverage is desired. We have demonstrated the feasibility of depositing such profile by balancing deposition, surface diffusion, and film resputtering using the Lam

hollow cathode magnetron (HCM®) PVD source. Necessary conditions were obtained by utilization of extremely low operating pressure, Cu self-sputtering, and strong magnetic confinement of plasma in the entire volume of the deposition module. The novel configuration of the magnetic field ensured that the metal ion/neutral ratio was uniform across a 300mm wafer. With the proper metal ion/neutral ratio, more than 70% of the volume of a small feature could be filled while larger features were lined with Cu film. Thus, the aspect ratio of small features was significantly reduced, resulting in void free electrofill. PVD film is characterized by small grains which attribute to high resistivity, especially inside small features. We demonstrated that the grain size can be increased with post-deposition anneal, which resulted in improved line resistance. Deposition in very large CD and AR features, such as through-silicon vias (TSV), benefited as well. The metal ion-rich deposition formed a continuous seed on the TSV sidewall with 3-5 times less flux required than with standard PVD.

4:00pm **EM-ThA7 Analysis of Grain Structure and Electrical Resistivity of 17 nm Half-Pitch Copper Wires**, ***J.S. Chawla***, *K.J. Ganesh, B.J. Krist, J.S. Clarke, H.J. Yoo*, Intel Corporation

We report electrical resistivity, copper grain size, and grain orientation distribution for 17-51 nm drawn wires fabricated with Cu/Ta, Cu/Ru and CuMn/Ru based processes on 300 mm Si wafer platform. Interconnects containing those structures measured in this study were fabricated using patterning and metallization schemes described earlier [1, 2]. The grain structure and size are characterized using a recently developed technique [3, 4], which couples diffraction-scanning transmission electron microscopy (D-STEM) configuration with precession electron diffraction (PED). Electrical resistivity and *conducting* cross section area of each wire is obtained by a four-point probe resistance measurement at various temperatures (25-75 ^{o}C) and lengths of wire (25-100 μm). The *geometrical* cross sectional area is measured using transmission electron microscopy (TEM), and shows the *conducting* cross sectional area for both Cu/Ru and Cu/Ta wires equals the *geometrical* Cu cross-sectional area. This result indicates neither Ru or Ta liner contribute to conduction, owing to their high resistivity compared to Cu at these dimensions.

The wires studied for this report have a *conducting* cross-sectional area ranging from 150 to 1100 nm^2. The resistivity of Cu/Ru and Cu/Ta wires at *conducting* cross-sectional area of 200 nm^2 is 4.6 and 7.7 μΩ-cm, respectively. The resistivity of the Cu/Ru wire is 40% lower than that of the Cu/Ta wire, and can be attributed to a larger (2x) median Cu grain area for the Cu/Ru, thus resulting in reduced electron scattering at grain boundaries. The resistivity delta between Cu/Ru and Cu/Ta wires decreases from 3.1 μΩ-cm to 0.8 μΩ-cm as area increases from 200 nm^2 to 900 nm^2. This is attributed to a combination of respective increase in grain size, and reduction in electron scattering at surfaces with increasing dimensions. The resistivity of a CuMn/Ru wire with 200 nm^2 *conducting* cross-sectional area is 9.9 and 10.3 μΩ-cm with and without annealing, respectively. The higher resistivity for the CuMn/Ru wire is attributed to the Mn dopant, which increases impurity scattering. The electrical resistivity data is also consistent with the combined Fuchs-Sondheimer and Mayadas-Shatzkes expression.

References:

[1] M. van Veenhuizen et al., IEEE International Interconnect Technology Conference (IITC), 2012

[2] J. S. Chawla et al., IEEE International Interconnect Technology Conference (IITC), 2013

[3] K. J. Ganesh et al., *Microscopy and Microanalysis*, 16 (5), 2010

[4] K. J. Ganesh et al., *Nanotechnology*, 23 (13), 2012

4:20pm **EM-ThA8 The Role of Gas-phase Reaction during Co-CVD using Amidinate Precursor for ULSI-Cu Liner Application**, ***Y. Suzuki***, *H. Shimizu, T. Momose, Y. Shimogaki*, University of Tokyo, Japan

Reaction mechanism of chemical vapor deposition (CVD) for Co using amidinate precursor was examined by introducing multi-scale analysis using cold-wall reactor equipped with macrocavity. We thereby found that Co film growth by direct surface decomposition of the source precursor was negligible and the intermediate species generated by gas-phase reaction was the major species.

Ongoing shrinkage of ULSI devices manifests EM/SIV reliability issues originated from poor adhesion between Cu and underlying material. The higher effective resistivity caused by the shrinkage of Cu lines is another concern. These issues suggest the necessity of more adhesive and conductive material for Cu liner/barrier layer instead of conventional Ta/TaN bi-layer. We proposed Co(W) monolayer film as a hopeful candidate to solve these issues [1]. The poor step coverage of PVD is also a problem in future technology. We, therefore, worked on the CVD of Co(W), and proved better barrier property and lower resistivity than Ta/TaN. This paper is focusing on Co-CVD kinetics from $Co(^{t}BuNC(Et)NEt)_2$ (Co-amidinate) [2] and NH_3 as a basis of Co(W)-CVD.

We firstly used cold-wall chamber to focus on the surface reaction kinetics. Arrhenius plot of deposition rate showed two slopes corresponding to surface-reaction- and diffusion-limited regime. Mass transfer coefficient estimated from the growth rate under diffusion-limited regime has 200 times lower than that from fluid dynamics. This suggested that major deposition species was not the precursor itself, but intermediate species generated from the precursor near by the heated substrate. Deposition rate dependence on precursor partial pressure was then studied under reaction-limited condition, which showed Langmuir-Hinshelwood reaction kinetics. Surface reaction rate constants were finally extracted.

Gas-phase reaction kinetics were analyzed by macrocavity installed in the cold-wall chamber. Macrocavity consists of two facing substrates with variable spacing. The spacing of the macrocavity controls surface to volume ratio, which in turn changes the contributions of gas-phase reaction over surface reaction [3]. Film thickness profile within the macrocavity was compared with that by finite element simulation of diffusion equations coupled with the experimentally obtained surface reaction kinetics. We could finally obtained gas-phase reaction rate constant.

As a summary, we successfully analyzed reaction mechanism of Co-CVD using amidinate precursor, which enables to design the wafer-scale reactor. Our results show the importance of controlling gas-phase reactions when we use this precursor for CVD-Co as ULSI-Cu liner application.

4:40pm **EM-ThA9 Copper Reflow Modeling**, ***P. Stout***, Applied Materials

A copper reflow model implemented in a feature profile evolution model will be discussed. The barrier/seed/plating process flow is being challenged as the metal interconnects shrink in size. The barrier and seed deposition are requiring more of the total volume within the interconnect via and trench structures. Copper reflow is being explored as a means to fill via and trench structures for back end of line interconnects. The wafer is raised in temperature to allow copper to move, shift around, or "reflow" within the feature. The feature model used for the study is a 3D Monte Carlo model. The reflow model implemented here assumes Cu transport during reflow is due to surface diffusion. The surface diffusion depends on the wafer temperature, the material Cu is diffusing on (i.e., Cu, Ta, SiO2, etc.), and the local morphology of the surface. The implemented surface diffusion model is a hopping model. A probability matrix is constructed to determine the next surface "hop" location as the Cu moves around on the surface. The hopping Cu will settle into surfaces which minimize surface energy. In this model that translates to Cu preferring higher coordination number (CN) sites. Depending on the temperature and material parameters the minimal surface morphology can change. If hopping probabilities are similar between CNs the surface will roughen and become more dendritic. If there are large hopping probability differences the surfaces will become more faceted with low energy crystalline planes exposed. Using a simple hopping surface diffusion model, reflow behavior is shown. The model predicts the initial reflow causes rounding of the Cu surfaces and a shrinking of the opening as the surfaces round to a more minimal surface configuration. The end result for the successful reflow cases is a filled feature which is concave at the feature bottom or flat once the field is reached. The main issue with the reflow process is pinch-off at the feature opening causing void formation in the feature. For vias the model is predicting mostly void formation. One reason vias are more prone to void formation (vs trench) is the different CN distributions for a flat (trench) vs rounded (via) surface. Thus, the movement (i.e., hopping) of the Cu is different for these surfaces. Another reason is trenches are closing in on the opening from only two sides whereas the via is closing in from all sides. Once a void forms it is unlikely to breach the field and have more copper enter the feature. Smaller voids move more quickly about the feature vs large voids given the smaller amount of Cu needed to shift in the small void for the void center to change position.

5:00pm **EM-ThA10 Chemical Mechanical Polishing of Gold**, ***G. Karbasian***, *H. Xing, A.O. Orlov, P.J. Fay, G.L. Snider*, University of Notre Dame

In today's IC technology, the size of the transistors is constantly shrinking and interconnect RC delay is a dominant factor in determining the speed of circuits. Gold is a promising replacement for copper and aluminum due to its low resistivity and high chemical stability. A key feature of a successful Au CMP is the use of a relatively soft adhesion layer beneath the gold, along with proper slurry additives. Ni is a soft metal compared to other common adhesion layer metals such as Ti and Cr, and was therefore used as the adhesion layer. Ultra Sol A20 from Eminess Technologies Inc., an alumina based slurry with added potassium iodide, was used to polish the Au/Ni metal overlay on the patterned dielectric substrate. The slurry, at pH=4, was modified by adding hydrogen peroxide as an oxidizer.

Previously, Ishii et al.[1] observed that adding 30% H_2O_2 to an alumina based slurry with added potassium iodate at pH=4, in 1:1 ratio resulted in the maximum polish rate of gold, and proposed it as the optimum concentration. However, this slurry composition results in high static etch rate, i.e. chemical dissolution, of gold, approximately 95nm/min. This high static etch rate increases edge recess and dishing in the interconnect trench as shown in Figure1. Moreover, this concentration of H_2O_2 exceeds the optimal oxidizer concentration needed for the highest Ni removal rate[2]. The lower polish rate of adhesion layer compared to gold, which was lowest for Cr and highest for Ni due to their different hardness, made adhesion layer removal the limiting factor in determining the total polish time. Our experiments show that reducing the concentration of 30% H_2O_2 solution from 50% to 25% improves the selectivity between the adhesion layer and gold such that at this concentration, Ni is polished approximately 3 times faster than gold, and this allows us to reduce the total polish time by a factor of 3. Additionally, the chemical etch rate of gold dropped from 90nm/min to 30nm/min, which reduces the dishing of Au during the Ni removal step.

Adding SDS and PVP enhanced the stability of the colloidal slurry that was otherwise prone to agglomeration leading to nonuniform polishing and microscratches. A combination of H_2O_2 and UltraSol A20 in1:3 volume ratio along with added SDS and PVP resulted in a stable slurry giving a successful CMP Damascene process, Figure2, with 37nm of dishing across a 150 μm wide contact pad.

We have also studied the evolution of the coefficient of friction during the CMP process, and observed a decrease in this parameter when the metal overlay is polished away, suggesting that this can be used for end-point detection.

5:20pm **EM-ThA11 Effect of Nucleation Layer on Electrical Properties of W-contact in Sub 2x nm Flash Devices**, ***K.H. Lee***, *S.W. Kim, K.S. Lee, T.H. Kim, S.S. Lee, S.H. Kim, J.H. Won*, Samsung Electronics, Republic of Korea

With the continuous scaling down of integrated circuits, the diameter of a contact plug decreases. This causes an increase of contact plug resistance, which is not desirable for high-speed transistor operation. Since metal Tungsten (W) has good filling capability and electrical properties, it has been widely used in semiconductor device area such as gate, metal contact, and via. Tungsten deposition process consists of two steps of nucleation which is for seed layer and bulk step that is for contact filling by CVD process. B_2H_6 based W nucleation layer technology has been widely used to realize low resistive W film. [1,2]

In this study, the effects of W-nucleation layer using a B_2H_6 gas as a reducing agent of WF_6 gas on electrical properties of W-contact in sub 2x nm flash devices was investigated. CVD-W films using CVD reaction of WF_6 and H_2 gas were deposited on different thickness of nucleation layer. The resistivity of CVD-W film was not changed as thickness of nucleation layer increase because the thickness of nucleation layer is too thin to affect resistivity of CVD-W film. In order to decrease resistivity of CVD-W film, B_2H_6 treatment was carried out after nucleation process. It caused decrease of resistivity as B_2H_6 treatment cycle increased grain growth due to increase of grain size resulted from additional Boron atom. WF_6 reacts with absorbed boron preferentially causing a formation of β –W phase of amorphous phase W film which decelerates the nucleation with α -phase W film formed by H_2 reaction, which result in larger size grains and low resistive W film as B_2H_6 post-treatment cycle increases.

In addition, the resistivity of CVD-W deposited on three different thickness nucleation layers is not variable, which means the final grain size of CVD-W film is similar. The contact resistance increases (~12 %) when W nucleation cycle increases from x to x+4 cycles. In general, contact resistance on gate is associated with the resistivity of the total film stack related to final grain size. However, this result reveals that the resistivity of W nucleation layer also affects the contact resistance of CVD-W film although the resistivity of bulk-W film is dominant factor to define a contact resistance.

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Authors Index

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