Electronic Materials and Processing
Room: 101 B - Session EM-MoA

High-k Gate Oxides for High Mobility Semiconductors II
Moderator: A.C. Kummel, University of California San Diego

2:00pm **EM-MoA1 Silicene, an Option for Future Electronics**, ***A. Molle***, *D. Chiappe, E. Cinquanta,* CNR-IMM, Italy, *C. Grazianetti, M. Fanciulli*, Università degli Studi di Milano Bicocca, Italy **INVITED**

The silicon counterpart of graphene, the so called "silicene" [1,2], has been so far a theoretical option but its synthesis constituted a formidable challenge. Nonetheless, recent efforts have moved up this fascinating hypothesis to a concrete evidence [3][4] thus triggering a tremendous interest in silicene for electronic applications and fundamental investigations.

Non-trivial atomic arrangements of the silicene are expected to occur which are dictated by a delicate balance between planar and buckled bonding . Indeed, due to the large ionic radius of silicon, silicene is naturally prone to occur with a variety slightly-buckled configurations which can be driven by the silicene/substrate local interactions [1]. This structural complexity discriminates the experimentally observed silicene from graphene, and it is expected to bring basically new physical properties such as topological phase transitions, quantum spin Hall effect, or band gap opening [5]. Here we report on recent experimental results showing the formation of 2D epitaxial silicene on Ag(111) substrates [4] based on *in situ* scanning tunnelling microscopy-spectroscopy investigations.

Despite its structural flexibility, silicene is technologically limited by its chemical instability. Indeed, silicene undergoes oxidation when exposed to dry air. Then, interfacing silicene with a gate dielectric is essential for any feasible voltage bias application but also to barely save it from possibly destructive reactivity in ambient conditions.

While disentangling silicene from metallic templates is still an open challenge, on-top interface engineering of silicene is here addressed with the goal to develop a non-reactive encapsulation process. This effort enabled us to fabricate a chemically stable Al_2O_3/silicene/Ag heterostructure through a carefully tailored co-deposition of Al and O_2 [6]. Raman spectroscopy was then used to demonstrate the structural stability of the encapsulated silicene. Finally, new hints at Si nanosheets grown on *ad hoc* 2D material templates are also discussed aiming at the silicene "portability" for device-oriented exploitation.

These outcomes disclose exceptionally novel issues in the physics of the emerging silicene and promote a renewed interest in nanoscaled silicon as active material for electronic devices.

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2:40pm **EM-MoA3 Fabrication and Electrical Characterization of High-k/Germanium Tri Gate MOSFETs Grown by MBE on Bulk Silicon**, ***S. Anwar***, *C. Buie, C.L. Hinkle*, University of Texas at Dallas

Germanium has long been considered as a replacement channel material due to its higher intrinsic hole mobility compared to silicon and its relative compatibility with current CMOS processing. Growth of Ge channel materials on bulk Si would be ideal for minimizing cost and allow for the continued use of current manufacturing tools. Ge grown on Si, however, results in a significant defect density due to the 4.2% lattice mismatch, reducing device performance.

In this work, we study the fabrication of tri-gate Ge MOSFETs, grown by MBE, on Si using Aspect Ratio Trapping (ART) [1,2] to reduce the Ge defect density. ART is a growth technique that allows for the reduction of defects for lattice mismatched materials by trapping the threading dislocations into the sidewalls of patterned nanoscale trenches in which the epitaxial growth takes place. This technique has the added benefit of producing the necessary geometric structure required for highly scaled tri-gate devices, alleviating short channel effects, while simultaneously reducing defect density. The fabrication of high aspect ratio (>2) trenches in SiO_2 for epitaxial growth of Ge will be discussed as well as the issues and solutions associated with the inherent non-selectivity of solid-source MBE growth. TEM, SEM, and AFM are employed to characterize the growth quality and assess the various device fabrication steps.

Tri-gate MBE-grown Ge MOSFETs on Si are fabricated using a gate first process. A high-quality Ge interfacial region is obtained by a surface functionalization technique using 50 pre-pulses of DI-H_2O in an ALD chamber at 250°C, followed by a 2 nm thick interfacial Al_2O_3 deposition at 250 °C followed by a forming gas anneal (FGA) at 350 °C.[3] The FGA step converts the functionalized surface to a thin layer of GeO_2, improving the electrical characteristics of the devices. 2.5 nm of HfO_2 is then deposited by ALD followed by a 500 °C post-deposition anneal in N_2. 150 nm of reactively sputtered TiN is deposited as the gate metal. Schottky junction source and drain regions are formed by sputtering 20 nm of Pt, capped with TiN, and annealed at 400 °C to form $PtGe_2$.[4] A final 350 °C FGA completes the device processing. Detailed electrical characterization, using a suite of techniques, was performed and correlated with the MBE growth and gate stack formation.

This work is sponsored in part by the SRC Global Research Corporation.

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3:00pm **EM-MoA4 Sub 1-nm Ge-MOSFET with TiO_2/Al_2O_3 Gate Stacks and Interface Trap Passivation by Forming Gas Anneal**, ***L. Zhang***, *P.C. McIntyre*, Stanford University

Equivalent oxide thickness (EOT) scaling is one of the most critical challenges for future Ge-MOSFET technology. It is difficult to achieve sub-1 nm EOT with a single dielectric material, due to the intrinsic trade-off between dielectric constants and band gaps. Recently, bilayer high-k materials, such as TiO_2/Al_2O_3, HfO_2/Al_2O_3, have been paid increasing attention. However, there are several challenges remaining for bilayer high-k stacks on Ge substrate: 1) an ultra-thin high-quality GeO_2/GeO_x layer is generally reported to be necessary for effective Ge surface passivation, but this is difficult to obtain by routine thermal oxidation. It has been reported that processes such as post-dielectric deposition plasma oxidation are beneficial for preparing such interface layers. 2) The interface between the two high-k materials in the bilayer must be abrupt and their thicknesses well-controlled, to reduce gate leakage as the EOT is scaled. In this paper, we address these challenges by a simple, low-temperature process flow using thermal annealing. Using carefully-controlled atomic layer deposition (ALD) of the dielectric layers and a forming gas anneal (FGA), a TiO_2/Al_2O_3/Ge gate stack is demonstrated with EOT = 0.63 nm that achieves low D_{it} and gate leakage current density in MOS capacitors. Pt gated Ge-pMOSFETs with TiO_2/Al_2O_3 gate stacks are fabricated, and have a sub-1nm EOT, 75 mV/dec subthreshold swing, 10m A/m m on state current and avoid gate metal/TiO_2 reaction or interdiffusion.

In our process, a high quality Al_2O_3 layer on the Ge substrate is grown by atomic layer deposition with the help of efficient sites for $Al(CH_3)_3$ precursor adsorption produced by oxidant pre-dosing the Ge(100) surface prior to ALD. Forming gas anneal (FGA) is found to be a critical step to realize low interface trap densities in low EOT Ge transistors. We observed great improvement of device performance after FGA on both MOSCAPs and MOSFETs, the effectiveness of FGA determined by Al_2O_3 thickness, FGA conditions, and the identity of the overlying gate metal.

We have used both hard and soft x-ray synchrotron photoemission electron spectroscopy (PES) to investigate the Al_2O_3/Ge interface and the TiO_2 layer in various Al_2O_3/Ge and Pt/TiO_2/Al_2O_3/Ge structures before and after FGA. An increase in intensity of the Ge+4 feature is observed after FGA of Al_2O_3/Ge samples, and emergence of a detectable Ti +3 peak, consistent with loss of oxygen during FGA, is also identified in Pt/TiO_2/Al_2O_3/Ge samples. Effects of these local chemical changes on the MOS performance of the resulting gate stacks will be discussed.

3:40pm **EM-MoA6 Surface Passivation of III-V Antimonides and Ge Based MOSFETs**, ***K.C. Saraswat***, *S. Gupta, A. Nainani,* Stanford University, *B. Yang,* GLOBALFOUNDRIES U.S. Inc., *Z. Yuan*, Stanford University **INVITED**

Si CMOS scaling is reaching practical and fundamental limits. Currently, use of strain engineering to boost mobility is the dominant technology for high performance Si MOSFETs. However, mobility boosting by straining Si will also saturate with future scaling. Therefore, looking into future it becomes important to look at higher mobility materials like Ge and III-Vs

to continue scaling of MOSFETs. For these materials to become mainstream several problems need to be solved, including surface passivation. In this talk we will present our recent results on passivation of Ge, GeSn and III-V antimonides.

Ge and GeSn have recently emerged as promising candidates not only for high performance CMOS but also for optoelectronics. Ge PMOS with several different high-k dielectrics have been demonstrated with excellent performance. Ge surface passivation with GeO_2 shows low D_{it} near valance band (E_v). However, Ge NMOS have so far exhibited poor drive current. This is partially attributed to high D_{it} near the conduction band (E_c). In recent work we have achieved low and symmetric D_{it} through sulfur passivation followed by ALD of Al_2O_3 and then annealing in ozone. With these two treatments, a record-low D_{it} (<1E11/cm^{2}eV) at both band edges is achieved

In GeSn with increasing Sn content G valley comes down with respect to the indirect valleys, increasing population of electrons in this low electron mass valley which boosts mobility. A novel surface passivation scheme using ozone oxidation of thin Ge cap has been demonstrated with record low D_{it} of 3E10^{11}/cm^{2}eV at high-κ/GeSn interface.

While there have been many demonstrations on n-channel MOS in III-V semiconductors showing excellent electron mobility and high drive currents, hole mobility in III-V p-channel MOS has traditionally lagged in comparison to Si. GaSb is an attractive candidate for high-performance III-V pMOS due to its high hole mobility. Performance degradation due to interfacial traps is generally considered one of the main challenges for III-V MOSFETs. We have demonstrated passivation of GaSb with an ALD Al_2O_3 gate dielectric with a midband-gap D_{it} of 3E10^{11}/cm^{2}eV and demonstrated excellent pMOSFETs.

We have further investigated the suppression of interface state response using band engineering in III-V quantum well MOSFETs and experimentally verified the concept in antimonide compounds system using a gate-stack consisting of Al_2O_3/GaSb/InAlSb. It is shown that if the thickness of the interfacial layer of GaSb is scaled down to a few monolayers, the effective bandgap of the interfacial layer increases dramatically due to quantum confinement, which leads to the suppression of interface-trap response.

4:20pm **EM-MoA8 High-Carrier-Mobility p- and n-Type Field Effect Transistors Fabricated on Large-Area Wafer-Scale Ge Film Epitaxially Grown on Si**, ***S. Ghosh***, *S.M. Han*, University of New Mexico

Implementing a unique two-step simple molecular beam epitaxy (MBE) growth technique in our laboratory, we have successfully demonstrated heteroepitaxial growth of high-quality Ge on Si (GoS) that opens up a possibility for many applications, including high-mobility transistors integrated on Si substrates and high-speed, read-only memory using Ge as the channel material. We note that our Ge film covers the entire underlying Si substrate at the wafer scale without mesas or limited-area growth. However, the ultimate test of materials quality is device demonstration on engineered GoS substrates. Herein, we have investigated the characteristics of two such devices: p-MESFETs as well as p- and n-MOSFETs fabricated on GoS substrates. For p-MESFETs, we have measured a low-field peak effective hole mobility of 310 cm^2/V-sec and a cut-off frequency of 10 GHz at 200K. In this presentation, we will provide additional details of the device characterization. In addition to MESFETs, we have investigated electrical characteristics of planar p-MOSFETs fabricated on n-type GoS substrates. The defect density in n-type GoS obtained from etch pit density measurements is consistently below 1x10^6 cm^{-2}. p-MOS capacitors are first fabricated, using Ti/HfO_2/GeO_xN_y/n-Ge gate-stack structure. Angle-resolved X-ray photoelectron spectroscopy is employed to quantify nitrogen content within the GeO_xN_y layer. The corresponding gate leakage current density is below 10^{-3} A/cm^2 and D_{it} of 6x10^{12} cm^{-2} eV^{-1} at 300K. After characterizing p-MOSCAPs, we have fabricated p-MOSFETs from n-GoS substrates. In this work, a two-step thermally activated method, instead of ion-implantation, is used to define p+ doped source and drain. The sheet resistivity from Hall measurements supports the presence of p+ regions. Forward and transfer current-voltage characteristics are measured, and the p-MOSFETs built on GoS substrates show a subthreshold slope (SS) of ~100 mV/decade, compared to ~80 mV/decade for the identical p-MOSFETs built on Ge substrates. The effective peak mobility obtained from our optimized p-MOSFETs is 401 cm^2/V-sec. This is an 82% increase in the effective carrier mobility in the inversion channel in GoS, compared to the universal effective hole mobility in Si. In summary, a wafer-scale, epitaxial Ge layer on Si is used to fabricate high-hole-mobility p-MESFETs and p-MOSFETs. In this talk, we will further discuss n-MOSFETs fabricated on p-type GoS substrates, exploring the possibility of fabricating high-carrier-mobility CMOS devices from GoS substrates.

4:40pm **EM-MoA9 Passivation, Functionalization, and Atomic Layer Deposition Nucleation of SiGe(100) via H_2O and H_2O_2**, ***T. Kaufman-Osborn***, *A.J. Kerr, A.C. Kummel*, University of California, San Diego

Silicon-germanium is a promising candidate for potential channel or contact materials due to its higher hole and electron mobility. To minimize the oxide-semiconductor interfacial defect density, a chemical and electronic passivation layer must be formed before the oxide layer is deposited. In this study, a monolayer of H_2O or H_2O_2 chemisorbates is shown to activate Trimethylaluminum (TMA) chemisorption due to the Si/Ge-OH bonds catalyzing the formation of an ultrathin passivation layer which can serve as an ideal ALD nucleation template on SiGe. However, since H_2O chemisorption results in equal density of Si/Ge-H and Si/Ge-OH sites on the SiGe(100), H_2O can only provide a maximum of 0.5 monolayer of Si/Ge–OH sites, limiting the TMA nucleation density. By using H_2O_2 dosing, the density of Ge–OH sites can be doubled thereby increasing the potential TMA nucleation density. This study compares the passivation of the SiGe(100) surface via H_2O and H_2O_2, for the application of nucleating ALD growth on the surface, using scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and x-ray photoelectron spectroscopy (XPS).

Using a differentially pumped dosing system, a clean SiGe(100) sample was dosed at room temperature with a saturation dose of either H_2O or H_2O_2. STM and XPS measurements indicate that H_2O_2 dosing leaves the SiGe(100) surface, which is mostly Ge atoms due to surface segregation, terminated with an ordered monolayer Ge-OH sites. A very small density of unreacted atoms are left unpassivated on the surface and have half filled dangling bond states causing a large local amount of conduction band edge states in the bandgap. STS measurements of the Ge-OH sites show the conduction band edge dangling bond states are eliminated due to the passivating Ge–OH bonds, but the Fermi level is pinned near the valence band edge due to the large surface dipole . When the surface is annealed to 310°C, XPS measurements indicate that the –OH species on the surface break bonds with the Ge atom and bond instead to the Si atoms, raising Si atoms towards the surface. XPS also verifies that no oxygen leaves the surface due the 310°C anneal. Instead, the oxygen remains on the surface in the form on Si-OH or SiO_x species. It is hypothesized that a lower temperature anneal would prevent SiO_x species from forming, leaving a surface which is only terminated by Si-OH bonds which would serve as an ideal template for ALD nucleation of TMA for Al_2O_3 growth. STS measurements show that TMA nucleation on the H_2O_2 functionalized SiGe(100) surface unpins the Fermi level and has a wide bandgap with no band edge states demonstrating very good interface quality.

5:00pm **EM-MoA10 III-V on Insulator (XOI): Processes, Materials, and Devices**, ***A. Javey***, University of California at Berkeley **INVITED**

Two-dimensional (2-D) semiconductors exhibit excellent device characteristics, as well as novel optical, electrical, and optoelectronic properties due to quantum size-effects. In this talk, I will discuss layer transfer of single crystalline III-V semiconductors with nanoscale thicknesses on Si/SiO2 substrates. The resulting III-V-on-insulator (XOI) substrates enable the exploration of a wide-range of device applications, while allowing for fundamental science exploration of the carrier properties as a function of thickness, without the constraints of the original growth substrates. Specifically, the quantized sub-bands of ultrathin III-V membranes (3-20 nm in thickness) are directly visualized by optical absorption studies. The measured effective bandgap is shown to increase by ~3x for InAs XOI as the layer thickness is reduced to ~3nm. Through experiments and modeling, we demonstrate the drastic role of carrier quantum confinement on the contact resistance and carrier transport properties of field-effect transistors (FETs). These results provide an important advance towards establishing the fundamental device physics of 2-D semiconductors. Additionally, high performance InAs and InGaSb complementary XOI-FETs are fabricated on Si substrates with electron and hole mobilities of ~4000 and 800 cm2/Vs, respectively. This presents the first III-V CMOS demonstration. Overall, the results shed light on the performance limits of III-V ultrathin body FETs.

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