Electronic Materials and Processing
Room: 102 A - Session EM+PS-WeM

Oxides and Dielectrics for Novel Devices and Ultra-dense Memory II
Moderator: J. Kim, The University of Texas at Dallas

8:00am **EM+PS-WeM1 Active Surfaces and Interfaces in Valence Change Memory Type Oxides**, *R. Waser, R. Dittman,* RWTH Aachen University, ***C. Lenser***, Forschungszentrum Juelich GmbH, Germany **INVITED**

Flash memories and DRAM are ubiquitous today. However, a potential leap beyond the limits of Flash (with respect to write speed, write energies) and DRAM (with respect to scalability, retention times) emerges from nanoionic redox-based switching effects encountered in metal oxides (ReRAM). A range of systems exist in which ionic transport and redox reactions on the nanoscale provide the essential mechanisms for memristive switching. One class relies on mobile cations which are easily created by electrochemical oxidation of the corresponding electrode metal, transported in the insulating layer, and reduced at the inert counterelectrode (so-called electrochemical metallization memories, ECM). Another important class operates through the migration of anions, typically oxygen ions, towards the anode, and the reduction of the cation valences in the cation sublattice locally providing metallic or semiconducting phases (so-called valence change memories, VCM). The electrochemical nature of these memristive effects triggers a *bi*polar memory operation. In yet another class, the thermochemical effects dominate over the electrochemical effects in metal oxides (so-called thermochemical memories, TCM) which leads to a *uni*polar switching as known from the phase-change memories. In all systems, the defect structure turned out to be crucial for the switching process.

The presentation will cover fundamental principles in terms of microscopic processes, switching kinetics and retention times, and device reliability of the VCM-type ReRAM variant. It will describe what can be learnt about the nature of the redox-based switching process on open surfaces (e.g. system with top electrodes removed) and embedded electrode interface.

Despite exciting results obtained in recent years, several challenges have to be met before these physical effects can be turned into a reliable industrial technology.

8:40am **EM+PS-WeM3 Resistive Switching and Interface Structure of Metal / Ga_2O_3 / Metal Heterostructures**, ***B. Zhao***, *X. Zheng, H. Pham, M.A. Olmstead, F.S. Ohuchi*, University of Washington

Materials exhibiting reversible resistance changes are essential elements of resistance random access memory (R-RAM), which has a simpler structure, lower energy consumption, higher operating speed and higher endurance than conventional RAM. The monoclinic transparent conducting oxide β-Ga_2O_3 is a promising candidate for R-RAM due to its open-channel structure that enables large scale defect migration. The resistive switching mechanism in pulsed-laser-deposited Ga_2O_3 was investigated by combining electrical measurements with x-ray diffraction (XRD) and sputter-profiling x-ray photoemission spectroscopy (SP-XPS), revealing a strong correlation of oxide-metal interface conductance with electrically and thermally driven defect migration and agglomeration near the interface.

Electrically-activated reversible resistance switching is observed in thin-film Ni/Ga_2O_3/Ir, while irreversible changes can be observed upon annealing either single-crystal or thin film gallium oxide. Room-temperature Ni deposition on single crystal β-Ga_2O_3 results in a rectifying contact with barrier height ~ 0.8 eV and SP-XPS reveals no interface reaction; annealing this structure to 500°C irreversibly creates an ohmic contact, as well as oxidized Ni and reduced Ga at the interface.

A reversible resistance change can be triggered by an electrical pulse in polycrystalline gallium oxide films grown by pulsed laser deposition. Ni/Ga_2O_3/Ir heterostructures were fabricated and then investigated at different points in their electrical cycling history. Application of less than about 10 V across a 100 nm film (~10^6 V/cm) maintains the initial Schottky behavior; a 1 sec, 30 V electric pulse switches the metal/oxide contact from Schottky to Ohmic and increases the device conductance by two orders of magnitude. X-ray diffraction shows the film recrystallizes into α and β phases of Ga_2O_3; further electric field treatment increases the β-phase fraction. Sputter-profiling XPS shows an increase in the near-surface Ga:O ratio and introduction of reduced Ga within 2 nm of the metal-oxide interface. The film remains Ohmic under low voltage cycling, but a high-voltage pulse with the opposite polarity both reverses the interface chemical changes and reverts the electrical characteristic to a Schottky contact. Further cycling between Ohmic and Schottky behavior continues with additional voltage pulses. The results are consistent with Ga interstitial migration and/or an interface redox reaction.

This project is supported by the National Science Foundation under DMR 1104628 and the Micron Foundation.

9:00am **EM+PS-WeM4 The Effect of High-Pressured N_2 Annealing in NiO_x based Resistive Random Access Memory**, ***D.H. Yoon***, *Y.J. Tak, J. Jung, S.J. Kim, H.J. Kim*, Yonsei University, Republic of Korea

High pressure annealing (HPA) is known as an effective way to control the fundamentals of oxide system through the modification of stoichiometry, thermal decomposition, and compression.[1] Here, we report the effect of N_2 HPA on NiO_x based resistive random access memory (RRAM) device in terms of applied pressures in NiO_x system. In this research, the annealing temperature was fixed at 350 °C while the applied pressures were varied to 1, 20, and 50 atm. Pt was commonly used as bottom and top layer of metal-insulator-metal structure. As the N_2 pressure increased, the on- and off-resistance ratio was decreased from ~10^5 to ~10^4. However, the operation voltages (reset and set voltage) were reduced followed by increment of N_2 pressure. Specifically, the 50 atm HPA sample shows the lowest reset voltage of 0.95 V and set voltage of 2.12 V. This result implies that enhanced grain size was induced by the N_2 pressure as the grain boundaries are preference sites for conduction filament formation.[2] Furthermore, notable increment of non-lattice oxide component was confirmed which may cause the reduced driving voltages by x-ray photoelectron spectroscopy. These findings can enhance the understanding of low-power driving RRAM for next generation memory device.

References:

[1] Y. S. Rim, W. H. Jeong, D. L. Kim, H. S. Lim, K. M. Kim and H. J. Kim, J. Mater. Chem. **22**, 12491 (2012).

[2] S. Kim, D. Lee, J. Park, S. Jung, W. Lee, J. Shin, G. Choi, and H. Hwang, Nanotech. **23**, 325702 (2012).

9:20am **EM+PS-WeM5 Ionic Memory - Materials and Devices**, ***M.N. Kozicki***, Arizona State University **INVITED**

There is widespread agreement within the semiconductor industry that existing high density non-volatile memory technologies are reaching their scaling limits and will ultimately be replaced by some variant of resistive random access memory (RRAM). This paper discusses advances in ionic RRAM, which relies on ion transport and redox reactions in thin solid electrolyte/dielectric films. Emphasis is placed on a technology known as Conductive Bridging Random Access Memory (CBRAM), a recently commercialized ionic memory based on the Programmable Metallization Cell (PMC) platform. In this technology, metallic cations are typically the mobile species. An ion current will flow if (1) the electrolyte is placed between two conductive layers, at least one of which can supply ions, (2) the ion-supplying electrode is made positive with respect to the opposing electrode, and (3) a sufficient bias is applied to overcome the internal potential barrier. The ion current feeds the reduction reaction, resulting in the formation of a metallic filament within the electrolyte/dielectric. The filament has a conductivity that is much higher than the surrounding material and hence it allows the resistance of the structure to be reduced by several orders of magnitude. The resistance of the conducting filament depends on the total number of metal ions that are reduced, which in turn depends on the charge supplied by the external circuit. Thus, the on-state resistance can be controlled by programming current and time. Control over the on-state resistance means that it is possible to create multiple discrete resistances levels to represent more than one binary digit per cell. If one electrode is electrochemically inert, the resistance-change process can be reversed by applying an opposite bias to that used for programming which dissolves the conducting pathway via oxidation of the metal in the filament. It is this electrode asymmetry that allows the deposition/dissolution process to be cycled repeatedly. We have also studied stackable diode-isolated arrays, in which each cell has one resistive switching element and one integrated Zener diode formed by the junction of the Cu filament of the device on-state and a doped silicon (n-type) electrode. The diode reduces "sneak path" currents via low resistance on-state devices in an array, but the reverse breakdown of the Zener element allows the cells to be erased by reverse bias.

10:40am **EM+PS-WeM9 Electrode-bias Injection and Percolation Controlled Transport through Vacated O-atom Site Defects in Nano-grain (ng-) TM Oxides and in Non-crystalline (nc-) Si(Ge)O_2**, ***D. Zeller****, G. Lucovsky,* North Carolina State University*, J. Kim*, University of Illinois at Urbana Champaign

Remote plasma CVD of thin film (i) non-crystalline nc-SiO_2 on Si substrates and (i) nanograin ng-TM oxides thin-film dielectrics plasma processed Ge substrates combined removal of Ge-O and Ge-N layers by post-processing annealing presents new opportunities for devices.

Semiconductor conduction band edge states (CBES), and symmetries and singlet transport and/or trapping states of vacated O-atom defects are quantitatively different for nc-Si(Ge)O_2 and nano-grain (ng-) TM oxides. CBES in Si(Ge)O_2 and Si/Ge an zinc-blende III-V semiconductors are "s-like" with high electron mobilities. Combined with intrinsic band edge triplets in SiO_2, energies of vacated O-atom singlet defect states are deeper into the band-gap. Injection into, and transport through singlet defects localized in 1 nm nc-SiO_2 clusters with "crystalline-like" medium range order (MRO) extends to self-organized symmetric dihedral angles. Hopping transport through vacated O-atom sites is determined by percolation. It is l\eiminated through nc-Si(Ge)O_2 interfacial transition regions by the 0.6 eV spectral extent of the intrinsic band edge triplets explaining the absence of bulk negative space-charge in devices, and after accelerated bias-controlled stress testing. CBES and vacated O-defects in X-ray absorption spectra (XAS).

Properties of nc-SiO_2 dielectrics and their semiconductor interfaces are the standard against which high-k TM gate dielectrics are evaluated. CBES are "d-like" with symmetries dependent on coordination, "t_{2g}-like" for 6-fold coordinated TiO_2 and Ti_2O_3 and Magneli-phase alloys, and "e_g-like" for 7- and 8-fold coordinated HfO_2 and ZrO_2. Jahn-Teller effects remove 3-fold t_{2g} and 2-fold e_g degeneracy in O K-edge XAS in thin films <2 nm in TiO_2 and <3 nm-HfO_2.

In thicker films O-vacancy singlet states are below CBES with bias-controlled injection and transport. Combined with metal gates, and n- and p-type doping, for Si, Ge and III-V semiconductor substrates, memory and switching functionality is established. 300° CVD devices are obtained in RPD ~2 nm thick TiO_2 or HfO_2 onto nitrided Ge substrates with ~0.5 nm of Ge-N detected by in-line AES. 400-500°C post-deposition annealling removes Ge-N bonds at nitrided interfaces, and provides a template for deposition of nc- and ng-dielectrics. Nc-HfSiON on Si-passivated and nitrided Ge (100) and ng-TiO2 yield Dit levels of 2-5x10^{10} cm^{-2}. C-V characteristics are symmetric with respect to flat-band voltages, V_{FB} yielding fixed charge levels ~2-3x10^{11} cm^{-3}. J-V characteristics yield currents at 1 V > $V_{FB,}$ of 3-5x10^{-6} A-cm^{-2}. TiO2 capacitors on Ge have EOT values of ~ 4.5 nm, as well as low values of Dit .

[1] G. Lucovsky, et al: Many-Electron Multiplet Theory Applied to O-Vacancies in (i) Nanocrystalline HfO2 and (ii) Non-crystalline SiO2 and Si Oxynitride Alloys, Progress in Theoretical Chemistry and Physics 23 (2010) 193-211.

[2] G. Lucovsky, D. Zeller, Remote Plasma Enhanced Chemical Deposition of Non-Crystalline GeO2 on Ge and Si Substrates, Journal of Nanoscience and Technology 11 (2011) 7974-7981

[3] Y. Tanabe, S. Sugano, On the absorption spectra of complex ions, Journal of the Physical Society of Japan (1956) 11 (8) (1956) 864–877; 9(5) (1954) 9(5) 766-779.

11:00am **EM+PS-WeM10 Investigation of the Dominant Conduction Mechanisms in Metal-Insulator-Metal Tunnel Diodes with Ta_2O_5 and Nb_2O_5 Dielectrics Deposited by Atomic Layer Deposition**, ***N. Alimardani****, J.F. Conley, Jr.*, Oregon State University

Thin film metal-insulator-metal (MIM) tunnel devices have seen renewed interest for high speed applications such as infrared (IR) detectors, optical rectennas for energy harvesting, and hot electron transistors. For many of these applications, desired properties include high asymmetry (η) and non-linearity (f_{NL}) of current vs. voltage (I-V) behavior and small turn-on voltage (V_{ON}). The standard approach to achieving these characteristics in tunnel devices is M_1IM_2 diodes - the use of electrodes with different workfunctions to induce a built-in field across the insulator. V_{ON} is influenced by the choice of the dielectric layer. In theory, small band-gap dielectrics with large electron affinity (χ) are desired to achieve small V_{ON} in tunnel diodes as they make small energy barriers with electrodes. Regarding this, Nb_2O_5 and Ta_2O_5 are widely considered to be promising candidates as tunnel dielectrics. In this work, we investigate Nb_2O_5 and Ta_2O_5 MIM diodes. Atomic layer deposition (ALD) was used to deposit 5 nm and 10 nm thick Nb_2O_5 and Ta_2O_5 tunnel barriers with sputtered amorphous bottom electrodes (ZrCuAlNi) and evaporated Al top electrodes. The I-V responses were found to be asymmetric for diodes made with 5 nm and 10 nm of either of these dielectrics. Although a lower V_{ON} was observed, the maximum asymmetry was 3 orders of magnitude smaller than what we previously reported for similar diodes with ALD Al_2O_3 as the dielectric layer. High speed operation of MIM devices is typically based on Fowler-Nordheim tunneling (FNT). Conduction mechanisms were investigated as a function of temperature and electric field. By fitting I-V curves to FNT, Schottky emission (SE), and Frenkel-Poole (FP) emission plots, the dominant conduction mechanism in these diodes was found to be SE in the small bias regime (0.1 V to 0.3 V) and FP emission in the large bias regime (≥ 0.75 V). These assignments were confirmed by the close match of the optical dielectric constants extracted from the SE and FP plots with spectroscopic ellipsometry. Finally, Arrhenius plots show temperature dependence of current at both small and large bias regimes, indicating that tunneling is not the dominant conduction mechanism. In conclusion, we find that the small low-voltage asymmetric I-V behavior in MIM diodes made with Nb_2O_5 and Ta_2O_5 dielectrics is due to SE, rather than FN tunneling. A comparison will be made to bi-layer dielectric MIIM diodes, which we recently reported to show improved low voltage η and f_{NL}. This work indicates that the choice of dielectric is critical as high χ dielectrics may not exhibit conduction mechanisms appropriate for high speed applications of MIM tunnel diodes.

11:20am **EM+PS-WeM11 Mechanism of Light Emission and Optical Characteristics of Thin Film Metal Oxides**, ***Y. Kuo****, C.-C. Lin*, Texas A&M University

Currently, light emitting devices (LEDs) are made of inorganic or organic semiconductor materials prepared in crystalline thin films or nanocrystalline dots. They usually emit narrow band light due to the limit of the band gap energy of the semiconductor material. Commercial p-n junction or quantum well LEDs are fabricated with the MOCVD process involving toxic chemicals on the expensive single crystal substrate. Compared with the incandescent or the fluorescent light bulb, these LEDs have many advantages, such as the compact size, long lifetime, and low power consumption, but at the expense of the higher price, e.g., by more than one order of magnitude. On the other hand, the good-quality white light cannot be emitted from a single LED chip. It requires a set of three different LEDs or one LED in combination with a phosphor layer.

Recently, it has been reported that the broad band white light could be emitted from a new type of LED that has a MOS structure with a very thin amorphous metal oxide high-*k* dielectric layer (1,2,3). The complete device can be easily fabricated on the Si wafer using the IC compatible process at a low thermal budget. In this talk, authors will discuss 1) the light emission mechanism, which is from the thermal excitation of the conductive paths formed during the dielectric breakdown, 2) the optical characteristics, which covers the whole visible and part of the IR wavelength range of 400 nm to 1,000nm with a high color rendering index of 95, and 3) the lifetime, which is longer than 1,500 hours under the continuous operation at room temperature in the air. The unique physical structure and material properties of the sub 10 nm thick metal oxide layer are responsible for the light emitting phenomenon. Experimental results on this kind of device will be shown and discussed. In summary, this type of LED is applicable to a large range of industry, consumer, medical, etc. products.

(1) Y. Kuo and C.-C. Lin, *Appl. Phys. Lett.,***102**, 031117 (2113).

(2) Y. Kuo and C.-C. Lin, *ECSSolid State Lett.*, **2**(8) Q59-Q61 (2013).

(3) Y. Kuo and C.-C. Lin, Solid State Electronics, accepted, August 2013.

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