Electronic Materials and Processing
Room: 101 B - Session EM+PS-TuM

High-k Oxides for MOSFETs and Memory Devices I

Moderator: A.C. Kummel, University of California San Diego

8:00am **EM+PS-TuM1 Calibration of Capacitance Force Microscopy using Micro-scale Gold Dots**, ***K. Sardashti***, *A.C. Kummel*, University of California San Diego

Capacitance force microscopy (CFM) is a variant of atomic force microscopy (AFM) and a powerful tool in characterization of metal-oxide-semiconductor capacitors (MOSCAPs). A high accuracy CFM system can be built by modifying a commercially available AFM, connecting the tip and sample to capacitance bridge of tunable frequency. The electric field distribution and, as a result, minority carriers' response to the applied bias strongly depend on the contact area between the gate and oxide. Furthermore, the frequency dependence of the capacitance-voltage measurement (C-V) is a function of the electrode size due to the radial diffusion of minority carriers near the periphery of the electrode as the dimension shrinks to the size of AFM tips. Therefore, contact area between the tip and sample is a crucial factor in CFM measurements. An experimental method is required to determine the effect of contact area on the shape and frequency-dependence of C-V curves measured by CFM. Scanning capacitance calibration samples are being fabricated with gold dots of diameters ranging from 2 to 600 μm on heavily doped silicon with 100 nm thick SiO_2 grown on top. The capacitance of resulting $Au/SiO_2/Si^+$ stacks with a 90000x range of area will be measured both by a conventional probe station (Agilent B-1500) and a CFM system (Veeco Multimode® connected to an AH 2700A capacitance bridge). After calibration, second set of samples including gold dots of similar size on Al_2O_3 layers, grown by atomic layer deposition (ALD), on GaN substrates will be characterized by both the probe station and CFM systems.

8:20am **EM+PS-TuM2 RF-PVD Si Capping for CET Decrease in High-h/Metal Gate 14nm FDSOI**, ***C. Suarez Segovia***, *P. Caubet*, STMicroelectronics, France, *C. Leroux*, CEA-LETI, France, *M. Juhel, S. Zoll, O. Weber*, STMicroelectronics, France, *G. Ghibaudo*, IMEP-LAHC, France

Further miniaturization of CMOS technologies will require low values for Capacitance Equivalent Thickness (CET) of gate dielectrics. Below 28nm node, it becomes more difficult for high-k/metal gate (HKMG) MOSFET to reach low CET without degrading gate leakage. One technique for CET scaling already reported [1-4] is based on oxygen scavenging from the HKMG stack after thermal treatment (drive-in anneal). Unlike other reported CET scaling solutions, oxygen scavenging is a promising approach to extend Hf-based HK dielectrics to future nodes [2].

Scavenging techniques incorporating the scavenging elements such as Hf, La, Ti, Al, and Ta directly within the high-k layers have been proposed by many researchers [2-3]. However, this approach can present several drawbacks such as excessive carrier mobility degradation, leakage current increase and effective work function change by formation of fixed charges and/or interface dipoles [3].

In this study, in-situ RF-PVD Si-cap was deposited on top of metal gate in an Applied Materials Endura chamber. HfO_2 and TiN metal gate were used on 300mm FDSOI wafers, using a gate-first integration scheme in a 14nm process flow. The use of an in-situ Si-cap for achieving CET reduction has already been reported in the literature [4]; but, for the first time in this article, we have evaluated a new RF mode PVD Si-cap process, designed to avoid device degradation due to charging.

Firstly, SIMS and XRD measurements were carried out on blanket wafers containing either 20Å or 100Å thick RF-PVD Si-cap deposited in-situ on sacrificial 35Å TiN layer followed or not by drive-in anneal. SIMS results show that amorphous silicon is oxidized at TiN/Si-cap interface during drive-in anneal by pumping oxygen from TiN and high-k, which reduces CET. We demonstrate that Si-cap deposited by RF-PVD remains amorphous for both studied thicknesses whereas sacrificial 35Å TiN layer crystallizes after drive-in anneal, as indicated by XRD. We believe that oxygen diffusion through TiN is possible by means of the grain boundaries formed in TiN during annealing. Secondly, electrical measurements were obtained on 14nm FDSOI devices. As expected, with TiN capping by RF-PVD Si, we succeed to reduce CET by 1Å (6.25%) in PMOS and 0.5Å (4%) in NMOS with no significant degradation of the gate current leakage, no measurable impact on VT, and no device degradation due to charging.

[1] T. Ando et al.,Proceedings of IEEE IEDM, Washington,DC,USA 2009; pp. 423-426

[2] Takashi Ando, Materials 2012, 5, 478-500

[3] C. Choi et al J. Appl. Phys. 2010, 108, 064107:1-064107:4

[4] L.-Å. Ragnarsson et al, Proceedings of IEEE IEDM, Baltimore, MA,USA 2009; pp. 663-666

8:40am **EM+PS-TuM3 Growth of Oxides for Negative Capacitance Gate Dielectrics**, ***R. Droopad***, Texas State University **INVITED**

The need to reduce power in CMOS devices is critical to the evolution of the next generation devices as scaling continues. The use of new materials for the gate dielectric, and with the possibility of using III-V semiconductors in the channel, there is additional new challenges to maintaining high on-off ratios. One way to reducing the subthreshold slope in low power MOSFET application is through the use of the negative capacitance of ferroelectric layers as part of the gate dielectric proposed by Salahuddin and Datta [1]. This concept has been demonstrated in a polymer ferroelectric MOSFET device exhibiting a sub-60 mV/decade switching behavior [2]. Capacitance enhancement in crystalline ferroelectric-dielectric bilayer has also been demonstrated using a PZT-STO bilayer [3]. Unlike the present amorphous gate stack, ferroelectric gate materials need to be crystalline for the realization of polarization that is oriented along the growth direction. This presentation will detail the growth of ferroelectric complex oxide gate stacks epitaxially on both Si and III-V heterostructures. Deposition is carried out using MBE with careful control of the interfacial nucleation ensuring that the ferroelectric polarization is in the growth direction.

[1] S. Salahuddin, S. Datta, Nanolett. 8 (2008) 405.

[2] A. Rusu, G.A. Salvatore, D. Jiménez, A.M. Ionescu, IEDM 2010

[3] A.I. Khan , D.Bhowmik, P. Yu, S. J. Kim, X. Q. Pan, R. Ramesh, S. Salahuddin, Appl. Phys. Letts., 99 (2011) 113501

9:20am **EM+PS-TuM5 Switching Aspects of RRAM – First Principles and Model Simulations Insight**, ***S. Clima***, *R. Degraeve, K. Sankaran, Y.Y. Chen, A. Fantini, A. Belmonte, L. Zhang, N. Raghavan, L. Goux, B. Govoreanu, D.J. Wouters, M. Jurczak, G. Pourtois*, IMEC, Belgium **INVITED**

The Resistive Random Access Memory with its great potential for scalability to the nanoscale dimensions, high speed, low energy switching and CMOS compatibility, is emerging as a promising candidate for non-volatile memories.[1-4] Having a good understanding of the mechanisms at the origin of the switching at the atomic level is important for designing high performance resistive memory stack. For instance, the thermodynamic driving forces that help shaping a suitable oxygen profile for low forming voltages might prove to be disadvantageous for a good endurance. Another trade-off that needs further considerations is the compromise between the retention and the switching dynamics, determined by the kinetic energy barriers of the conducting defect. With the help of classical DFT and bond-boosted Accelerated Ab Initio Molecular Dynamics (AIMD) technique,[5] we evaluated the thermodynamics of the defects formation and the diffusion kinetics of the conducting species in RRAM materials.[6, 7] The experimental and first-principles outputs were used to develop a stochastic model simulator, which we use to interpret the experimental set/reset dynamics, endurance and retention measurements.[8] Modeling and simulations play an important role in understanding the atomistic mechanisms that take place during the manufacture, operation or storage of the resistive memory element. Through this talk we present our most recent advancements for oxide and Cu-based RRAM.

1. Z. Wei, et al., in *Electron Devices Meeting (IEDM), (2011)*, p. 31.4.1.

2. S. Shyh-Shyuan, et al., in Symposium on VLSI Circuits *(2009)*, p. 82.

3. L. Seung Ryul, et al., 2012 IEEE Symposium on VLSI Technology, 71 (2012).

4. B. Govoreanu , et al., Ext. Abstr. SSDM Conf.,Nagoya, Japan, pp.1005 (2011).

5. R. A. Miron and K. A. Fichthorn, Journal of Chemical Physics **119**, 6210 (2003).

6. S. Clima, et al., Applied Physics Letters **100**, 133102 (2012).

7. L. Goux, et al., in Symposium on *VLSI Technology (VLSIT), (*2012), p. 69.

8. R. Degraeve, et al., 2012 IEEE Symposium on VLSI Technology (2012).

10:40am **EM+PS-TuM9 Comparison of Surface Defects on Cleaved GaAs(110) and MBE Grown InGaAs(110)**, ***M. Edmonds***, *T. Kent*, University of California San Diego, *R. Droopad*, Texas State University, *A.C. Kummel*, University of California San Diego

The dominant crystallographic face of InGaAs(001) based FinFETs is the (110)surface. These sidewall surfaces do not have metallic group III bonds and therefore with proper passivation might provide ideal interfaces to the gate oxide. It has been shown shown that with trimethyl aluminum (TMA) passivation of GaAs(110), monolayer nucleation density with zero lattice disruption can be achieved which is ideal for sub 0.5nm EOT scaling. Furthermore, dual passivation with an oxidant such as $H_2O(g)$ has been shown to removes conduction band edge states associated with Al-Ga bonds results fromm TMA bonding. DFT studies confirm that TMA bridge bonds between the Ga and As atoms on the GaAs(110) surface while-OH from $H_2O(g)$ dual passivation can readily insert into the Al-Ga bond thereby unpinning the surface. This study focuses on examining and characterizing surface defects and features of cleaved GaAs(110) in comparison with molecular beam epitaxy (MBE) grown InGaA/InP(110) samples via scanning tunneling microscopy/spectrocscopy (STM/STS) studies. Models of the various surface defects are proposed.

The MBE grown InGaAs/InP(110) samples are grown with an As_2 cap in order to protect the surface from oxidation. The samples are decapped at 350°C in an ultra-high vacuum chamber system prior to STM imaging. The initial STM image results show the surface contains a much higher step density compared to cleaved GaAs(110). The STM images of MBE grown InGaAs(110) also shows bright site features which have an average height of ~2.5Å and a site width variation from 1.8 nm to 3.6nm. These bright site features are consistent with excess As on the surface from an incomplete decapping procedure, or from surface undercoordinated atoms. A commercially available thermal gas cracker will be used to expose the surface to atomic hydrogen. It is believed this will remove any excess As on the surface and potentially passivating instrisic surface defetcs . The dry in-situ atomic hydrogen cleaning of the MBE InGaAs(110) decapped samples will be compared with the cleaved GaAs(110) samples in aim to remove excess As_2 from the surface and make the InGaAs(110) surface comparable in low surface defect sites with cleaved GaAs(110).

11:00am **EM+PS-TuM10 Scalability of Doped Cubic HfO_2 Films**, ***C. Adelmann***, *K. Opsomer*, Imec, Belgium, *S. Brizzi, M. Tallarida, D. Schmeisser*, BTU Cottbus, Germany, *T. Schram, S.A. Chew, N. Horiguchi, S. Van Elshocht, L.-A. Ragnarsson*, Imec, Belgium

HfO_2 has been the standard gate dielectric for MOSFETs for several technology nodes because of its large dielectric constant (~18 for amorphous or monoclinic HfO_2). To continue MOSFET scaling, replacement dielectrics for HfO_2 are of interest with an even larger dielectric constant. The polymorphism of HfO_2 offers the possibility to increase the dielectric constant by stabilizing the cubic phase of HfO_2 with a dielectric constant of ~30. The stabilization of the cubic phase has been demonstrated by introducing dopants (typically about 10%) such as Al, Si, or rare earths.

Numerous studies have demonstrated the advantage of doped cubic HfO_2 over undoped HfO_2 in terms of leakage vs. equivalent oxide thickness (EOT) for films with thicknesses of ~5-10 nm. These stacks lead to EOT values >>1 nm and are thus not relevant for future CMOS technology nodes. However, no clear advantage has been shown for scaled films with EOT values <1 nm.

In this paper, we study the behavior of Gd- and Al-doped HfO_2 in capacitors with EOT values below 1 nm (physical thicknesses of 2-3 nm). While Gd- and Al-doped HfO_2 show similar leakage for 10 nm thick films, capacitors with 2.5 nm Gd-doped HfO_2 show several orders of magnitude higher leakage than their Al-doped counterparts, indicating that the behavior for thick and thin films is not correlated. However, EOT vs. HFO_2 thickness measurements show that dielectric constants of the order of 30 can be maintained even for 2.5 nm thick films.

The ultimate scaling limits were explored for Al-doped HfO_2. It was found that the scaling of Al-doped HfO_2 is limited by the crystallization temperature of the films, which becomes too large for acceptable temperature budgets for (gate-last) MOSFET processing for thicknesses approaching 2 nm. This was confirmed by x-ray absorption spectroscopy at the O K-edge. Thinner doped HfO_2 films remain amorphous and exhibit a lower dielectric constant. In-situ XRD showed that the crystallization temperature of thick films (10 nm) was increased significantly by Al-doping. However, for 2 nm films, the comparison with undoped HfO_2 led to similar crystallization behavior indicating that the effects of thin films and doping do not necessarily add up. The lowest EOT values that could be achieved for gate-last MOSFET compatible processing were of the order of 8 Å including an interfacial SiO_2 contribution of about 4 Å. However, for such stacks, leakage current densities could be achieved which were about 2 orders of magnitude lower than HfO_2 capacitors with identical EOT values. This indicates that doped HfO_2 films offer solutions for very low gate leakage at scaled EOT values down to values as low as 8 Å.

11:20am **EM+PS-TuM11 Advance of 3D-stackable Binary-oxide ReRAM for Storage-class Memory Applications**, ***T.H. Hou***, *C.W. Hsu, I.T. Wang*, National Chiao Tung University, Taiwan, Republic of China **INVITED**

Crossbar resistive-switching random access memory (RRAM) with a minimum cell size of $4F^2$ has attracted much attention recently because of its superior memory performance, ultrahigh density, and ultimate scaling potential. The most anticipating emerging application of RRAM in future high-speed information systems is the storage-class memory (SCM) aiming to revolutionize inefficient data-storage hierarchy based on hard disks and present memory technologies. The requirements of the SCM technology include high data bandwidth, large storage capability, and low bit cost.

Replacing the current 2D memory with 3D memory architecture is one of the most feasible options to further increase storage capability per unit area. The types of 3D memory architectures can be divided into the 3D stacking of horizontal memory arrays and the bit-cost scalable (BiCS) 3D vertical memory. In the first part of this paper, two crossbar RRAM architectures, namely one diode-one resistor (1D1R) and one selector-one resistor (1S1R) fabricated using low process temperature applicable to the 3D stacking of horizontal memory arrays, are discussed. Their high-bandwidth parallel read/write capabilities are also investigated.

Despite the increase of bit density, the formation of multiple horizontal memory arrays requires a larger number of photolithography steps, and thus is unable to reduce bit cost. By contrast, multiple layers of thin film deposition and a small number of photolithography steps are used to produce high-density 3D vertical RRAM arrays potentially at extremely low cost. Stacking two individual selection and memory devices as a 1D1R or 1S1R cell is extremely challenging in 3D vertical RRAM arrays because the metal electrodes between two devices cannot be easily patterned at the vertical sidewall. Therefore, it is of great interest to develop a nonlinear RRAM device requiring no external selection device. In the second part of this paper, the latest advance of self-rectifying devices compatible to 3D vertical RRAM arrays are reviewed.

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