Plasma Science and Technology
Room: 25 - Session PS2-TuM

Advanced FEOL/Gate Etching 2

Moderator: J.P. Chang, University of California at Los Angeles

8:00am **PS2-TuM1 Gate-Silicon Etching using Evanescent Microwave Plasma for 22nm Technology Node and Beyond**, ***A. Ranjan***, *S. Voronin, H. Kintaka, K. Kumar, P. Biolsi,* Tokyo Electron Technology Center, America, LLC, *R. Jung, S. Kanakasabapathy,* International Business Machines – Research Group, *A. Banik*, IBM T.J. Watson Research Center

Moore's law dictates continuation of shrinkage of transistors to make smaller, faster and less power-consuming devices at lower cost. FinFET (3-D) devices are needed to continue Moore's law. Anisotropy and selectivity requirements in FEOL etches (e.g., FinFET gate) are becoming very demanding and conventional RF plasma sources are hitting their limits to achieve such requirements. Microwave power delivered through radial line slot antenna generates over-dense evanescent microwave plasma just below top dielectric plate, and the electrons cools down (1eV or less in wafer region) due to inelastic collisions with the background gas. Low electron temperature (*Te*), low self-bias (Vdc) and low plasma potential in evanescent microwave plasmas enable "soft" etching for the 22nm generation and beyond technology nodes. In this study, Si-gate etching was performed in a evanescent microwave plasma system to achieve high selectivity over silicon oxide and silicon nitride with vertical profile. In addition to low self-bias, low *Te* is required to obtain high Si selectivity over SiO2 due to low-dissociation of by-products in evanescent microwave plasmas. Re-dissociated by-products (e.g., SiBrx*) pull out O- from SiO2 resulting in loss of Si selectivity over SiO2. Low *Te* (low re-dissociation) also helps with control of iso-nested CD-loading. High ion-flux with low *Te* plasma yields vertical profile of Si independent of aspect ratio and with minimal iso-nested CD-loading. Various other interesting aspects will also be presented.

This work was performed by the Research and Development team at TEL Technology Center America in joint development with IBM Research Alliance Teams in Albany, NY 12222. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

8:20am **PS2-TuM2 Tracking Line Width Roughness Improvement during Gate Plasma Patterning**, ***L. Vallier***, *E. Pargon,* CNRS, France, *N. Posseme,* CEA, LETI, MINATEC Campus, France, *L. Azarnouche,* CNRS, France, *S.D. Nemani, C. Rosslee, T. Pham*, Applied Materials Inc.

The effect of line width roughness (LWR) on the performance characteristics of transistor gates becomes problematic as the critical dimension (CD) of the gate decreases. Minimizing the magnitude of LWR in patterned features is becoming mandatory for the next technological nodes and is actually requested by the International Technology Roadmap for Semiconductor. Showing up particularly at 193nm wavelength exposure, the photoresist (PR) LWR is the main contributor to the final LWR measured in silicon gates following plasma patterning; therefore most of the effort is focused on the PR LWR reduction prior to the plasma transfer. At the same time, it was observed that the magnitude of LWR decreased when transferred from resist into the gate material. Plasma action might further help in the LWR reduction. In this work we have implemented the Power Spectrum Density (PSD) method as a measure of the LWR spatial frequencies distribution of a line, to monitor its evolution during the patterning of silicon gates with plasma etching process, starting from the PR after lithography up to the Silicon gate line. Thanks to the PSD method, noise coming up from CD SEM pictures of PR lines acquired at very low electron fluency can be subtracted, enabling a real LWR measure of the line with associated frequencies. A robust protocol for the CD SEM data treatment was developed and applied to various process conditions, aiming to obtain the best LWR reduction. Several cure treatment of the PR, achieved prior to the plasma etching of the gate, were investigated with the combination of UV light, plasma exposure using different gas chemistries, thermal treatment, pulsed plasma and E-beam exposure. This work confirms that the etch process can reduce the magnitude of roughness in silicon over a range of mid and high spatial frequencies, that is smoothing the line, however the extent of this roughness reduction vanishes as the resist LWR reaches its minimum. These results demonstrate that plasma action during the gate etch cannot improve the LWR much and post-etch LWR in silicon may be limited by the minimum LWR achievable in resist, therefore pushing for efficient PR cure treatment where plasma exposure play a key role. Based on the PR material used in this study which presents a 6.5 nm initial LWR value after lithography, a LWR of 2.9 nm was measured after the best LWR reduction process highlighting the need for further improvement to match the LWR requirement of the next technological nodes.

8:40am **PS2-TuM3 Plasma Prize Talk: Grand Challenges in Etch**, *R. Gottscho**, ***S. Sriraman***, Lam Research **INVITED**

Plasma etching has enabled the perpetuation of Moore's Law from >1 um to now less than 20 nm. More than ever, plasma etching is used to enable the extension of semiconductor device fabrication into the nanoelectronics age. The industry has always faced etch challenges due to scaling laws, especially as we begin to manufacture features that require atomic etch precision. Etch precision is especially challenging as the industry moves to 3D architectures, as we are etching electrically active layers in structurally complex features. Also, though we've always had to etch high aspect ratios, the fundamental challenge of aspect ratio dependent etching is now through alternating thin materials. The additional challenge to control wafer edge effects and reduce cost of consumables is ever more critical with compounding effects of multiple passes needed to compensate for lithographic limitations. In this presentation, I will give an overview of where we currently stand on our understanding of the origins and some solution approaches to the grand challenges in etch.

9:20am **PS2-TuM5 Spacer Patterning for Trigate SOI Devices**, ***S. Barnola***, *P. Pimenta-Barros, L. Desvoivres, J. Pradelles, S. Barraud*, CEA, LETI, MINATEC Campus, France

Demonstrations of Trigate SOI devices recently reported highlight a better scalability with improved subthreshold slope and immunity to short channel effect for aggressively scaled CMOS Si devices. However, there are several key challenges in these devices to achieve high performance. Extremely narrow and uniform silicon fins are required combined with increased fin pitch in order to improve the effective channel width and then, the drive current. This work aims to demonstrate Si fin pattern with a width of 10nm and a fin pitch of 35nm.It is no possible to create 10nm dense active features by using only 193nm immersion lithography because of its optical limitations. Consequently, several approaches have been developed in order to reach ITRS predictions, such as e-beam lithography, Extreme UV, negative tone development, block copolymer, and Self-Aligned Double Patterning (SADP). Regarding the technical issues that remain to be solved for each approach, SADP is one of the most promising solutions for the 14nm technology node and below.SADP approach includes at least 3 steps (lithography, spacer deposition, spacer and Si etching) to divide by 2 the pitch of the 1st lithography. For practical reasons and for reducing the number of SADP steps, e-beam lithography has been used to create the "mandrel" patterns that support the spacers. The e-beam initial pitch is 70nm, whose CD has to be reduced to 25nm by a trimming step to reach the final 35nm pitch after SADP. The integration scheme investigated in this work includes the following steps: e-beam lithography with trilayer stack, resist trimming, trilayer etching, SiARC removal, spacer deposition, spacer etching and SOC stripping. All plasma etching steps were carried out on 300mm ICP LAM VERSYS.One of the major challenges of this SADP integration was to limit the Si and SiO2 consumption from the SOI substrate during the SADP process steps. We also had to consider the impact of the non-symmetrical spacers on the micro-loading effect during Si etching. Integration scheme with a buffer layer has been investigated to limit the Si and BOX consumption, but this approach makes CD control more complicated. Thus, we have compared the two integration schemes, with and without buffer layer, in term of CD control and profile to achieve the requirements for this FEOL application for SOI technology.

9:40am **PS2-TuM6 Key Challenges in FinFET FEOL RIE Processing at the 14nm CMOS Node and Beyond**, ***R.M. Martin***, *A. Banik, J. Chang, R. Jung, S. Kanakasabapathy, M. Kobayashi, Q. Lin, B.G. Morris, S.C. Seo, T. Standaert, K. Stein, R. Sreenivasan, H. Wang, M. Yang, Q. Yang, Y. Yin,* IBM Corporation, *D.H. Choi, R. Kambhampati, T. Kwon*, GLOBALFOUNDRIES

For CMOS nodes at 22nm and below, the gate critical dimensions become small enough so that conventional methods for addressing issues such as short channel effects on planar devices become ineffective. Fortunately,

* 2011 Plasma Prize Winner

alternative non-planar devices are becoming mature enough so that they can be used at these next generation technology nodes. Development of new processes to build such three dimensional structures present new challenges for both lithography and plasma etching. In this presentation, we will review processes for building finFET devices in the front end of line (FEOL) from a patterning perspective. Below 80nm print pitch, double patterning methods such as sidewall image transfer (SIT) and pitch split can be employed, however, these more complex methods require additional precision in the plasma etching profile and selectivity to avoid issues such as pitch walking and line edge roughness. Furthermore, at these smaller dimensions and with the complication of 3 dimensions, issues such as RIE lag become much more apparent. Challenges such as these, and some of their potential solutions will be discussed.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

10:40am **PS2-TuM9 Patterning Options for 14nm Node and Beyond**, ***Y. Yin***, *R. Jung, F. Lie, M. Beard, B.G. Morris, M. Hartig, S. Kanakasabapathy*, IBM Res. at Albany Nanotech, *Y. Mignot*, STMicroelectronics, *Y. Xu, C. Koay*, IBM Res. at Albany Nanotech, *L. Jang*, GLOBALFOUNDRIES, *N. Saulnier, J. Abdallah, H. Chen*, IBM Res. at Albany Nanotech, *M. Tagami*, Renesas Electonics, *K. Akarvardar, S. Akarvardar*, GLOBALFOUNDRIES, *J. Arnold, T. Spooner, M. Colburn*, IBM Res. at Albany Nanotech

Beyond the 22nm node, limitations of traditional patterning processes become critical. Conventional 193nm immersion lithography is not able to resolve features below 40nm half pitch with a single exposure for Front, Middle and Back Ends of Line. Patterning vias at appropriate CD and spacing is equally challenging. Until further wavelength scaling through Extreme Ultraviolet (EUV) the industry's attention is focused on Double Patterning. Pitch Splitting (PS) Lithography and Sidewall Image Transfer (SIT) are the two broad categories of techniques that have been under evaluation for sub-22nm nodes. Moreover, as we keep shrink the key features to dimensions of interest to sub-14nm nodes, innovations on existing double patterning techniques and the introduction of emerging patterning techniques such as directed self-assembly are needed in order to enable sub-40nm pitch features patterning. In this talk we will address the innovations further needed on existing double patterning methods and discuss the opportunities and challenges of emerging advanced patterning techniques in order to meet the patterning requirements for 14nm node and beyond.This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

11:00am **PS2-TuM10 High-Efficiency Downstream Plasma Processes**, ***L. Diao***, *R. Elliston, A. Kadavanich, C. Lee, V. Nagorny, H. PhanVu, O. Todor, V. Vaniapura*, Mattson Technology

Photoresist (PR) strip processes continue to improve with major IC technology node advances and architecture changes. One of the new technologies currently being implemented for the 2x nanometer node, high-κ metal gate (HKMG) has emphasized the need for enhanced reducing chemistry processes, which are also widely used in other strip-over-metal applications. Three-dimensional vertical architectures present great challenges for high aspect ratio (HAR) processing, and stacked structures often require low-temperature process capability. Control specifications for critical processes are further tightened as more new materials are introduced at advanced geometries. Industry-wide strip process enhancements have diverged into two directions: increasing RF power or adding bias. In either case, wafer surface temperature increases significantly, which introduces pattern damage. Furthermore, there is increased risk of plasma-induced damage (PID). A new Mattson Technology dry strip source provides a solution to these challenges.

Based on the company's proprietory Faraday-shielded inductively coupled plasma (ICP) source technology, the new source offers these distinctive features: (1) a specially designed plasma generation volume with improved electron confinement that provides high efficiency of electron heating and enhanced plasma stability, and (2) a gas injection system that directs all the gas flow through this volume to increase efficiency of gas utilization. This results in efficient use of process inputs (power, gases) while simultaneously widening the operational window in terms of pressure, power, temperature.

The new source demonstrated significant increase of the PR removal rate and reduction of non-uniformity across different chemistries. One major benefit was observed with pure reducing chemistry. The new source with high power nearly doubled the ash rate, at 20% H2 in N2 with non-uniformity of <5%. Its impact on critical dimension (CD) and sheet resistance (Rs) were minimum and enabled better strip over metal process. O2-rich reducing chemistry with high power was used in HAR PR removal in the middle-end-of-line (MEoL) contact container. It showed improved residue removal capability with challenging AR. One more time, Rs was well controlled over exposed metal liner with high power. CF4-containing chemistry for amorphous carbon hard mask removal demonstrated improved productivity and selectivity over oxide and nitride at extremely low temperatures. Avoiding high power usage, the enriched reactant species allow HDIS process with dry only residue free, less pattern damage, lower silicon (Si) loss and controlled oxidation with different chemistries.

11:20am **PS2-TuM11 Challenges for Sub 20nm STI Etch**, ***H. Zhou***, *X. Ji, S. Srinivasan, J. He, X. Hua, D. Heo, J. Choi, A. Khan, A. Agarwal, S. Rauf*, Applied Materials Inc.

With the feature size scaled down below 20nm, the plasma etching technology for shallow trench isolation (STI) becomes very challenging. The aspect ratio of the isolation trench can be as high as 20:1, and the space CD variation from double patterning is no longer negligible. Advanced processes and hardware are then required for the sub 20nm STI etch to minimize the depth loadings, i.e. intra-cell loadings. First approach is to trim the mask at the beginning to reduce the aspect ratio of the mask. With trimmed mask, the intra-cell loading is reduced. Second approach is realized with pulsed plasma. The period of pulsed plasma is ~ms, which is comparable to the residence times of typical plasma etch conditions. During the off cycle, the radicals/ions/byproducts have extra time to move out of the trench or act on the sidewall independently, and the sidewall polymer deposition is better managed. The advantage of pulsed plasma has been demonstrated with both 13MHz and 2MHz bias frequencies. Synchronized pulsed plasma etching has shown at least 40% improvement on CD-dependent depth loading than continuous wave plasma process. Moreover, 2MHz bias frequency also helps to round the trench bottom with higher energized ions. Another challenge for sub 20nm STI etch is profile control at extreme edge. Because of the plasma sheath bending effect, extreme edge trenches tend to tilt toward the wafer center. This issue can be fixed with a novel improvement of bottom electrode, which also improves the depth uniformity across the wafer. The ion flux with the novel bottom electrode is more uniform, in particular at the extreme edge locations. Compared to the standard electrode, the center to extreme edge trench depth variation has been reduced from 14.55% to 4.42% with the novel bottom electrode. Challenges for sub 20nm STI etch also include in-situ etching and line bending prevention, which will be also discussed.

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