Thursday Morning, November 1, 2012

Plasma Science and Technology Room: 24 - Session PS1-ThM

Plasma Processing for Disruptive Technologies (NVM, TSV, etc.)

Moderator: S. Hamaguchi, Osaka University, Japan

8:20am PS1-ThM2 Damage Free Cryogenic Etching of Porous Organosilica Ultralow-k Film, L. Zhang, IMEC, Belgium, R. Ljazouli, T. Tillocher, P. Lefaucheux, R. Dussart, GREMI CNRS/Université d'Orléans, France, Y. Mankelevich, Moscow State University, Russia, J.-F. de Marneffe, S. de Gendt, M.R. Baklanov, IMEC, Belgium

Porous organosilicates (OSG) are popular candidates as low dielectric constant materials for interconnect application. However, the integration of this class of materials remains challenging, especially for $k \le 2.3$ materials with a large open porosity. Due to carbon depletion and surface modification, porous low-k materials suffer from plasma induced damage (PID) that leads to k value degradation and high leakage current. In this paper, we report a cryogenic low-k etching approach that benefits from a sidewall surface protection effect. It is known that, at cryogenic temperature, an SiO_xF_y passivation layer forms more easily on the surface of the material being etched, providing efficient sidewall protection. In this work, cryogenic etching is applied to porous organosilicate ultralow-k materials with k=2.3 and k=2.0, which are prepared by Spin-coating and PECVD methods respectively. Influence of the chuck temperature and bias power with different plasma chemistries has been investigated in an ICP chamber. Plasma induced damage is evaluated by means of spectroscopic ellipsometry (SE), Fourier-transformed infra-red spectroscopy (FTIR) and time of flight secondary ion mass spectroscopy (TOF-SIMS). Blanket low-k films are exposed to pure SF₆ plasma with different chuck temperatures, ranging from 20°C to -120° C. Almost no carbon depletion is observed when the chuck temperature is below a threshold point (-70°C and-120°C for k=2.3 and k=2.0 materials respectively). By addition of SiF₄ and O₂ to the gas discharge, etching rate is reduced as a result of enhanced SiO_xF_y polymerization. In order to evaluate the damage depth, an equivalent damage layer (EDL) is calculated based on the measurement of FTIR methyl group loss. The EDL decreases by increasing the proportion of SiF_4/O_2 in gas discharge, which confirms the protection effect of the SiO_xF_y passivation layer. In addition, the formation of alkyl alcohol polymer during cryogenic etching is observed from ex-situ FTIR, which is a major etch byproduct at cryogenic temperature due to the lack of activation energy for complete oxidation of the methyl groups into CO2 and H2O. Our experiments also show that this polymer can be easily removed by high temperature anneal without additional damage to low-k film. This incomplete oxidation of Carbon-based etch reaction products reveals the mechanism for reduced Carbon depletion during cryogenic etching. A protection model is proposed, for porous SOG etching at cryogenic temperature, based on SiO_xF_y growth and incomplete oxidation. Although the etch by-products cannot plug the interconnected pores, they condense on their surface and retard the oxidation of methyl groups.

8:40am **PS1-ThM3 Deep GaN Etching : Role of SiCl₄ in Plasma Chemistry, J. Ladroue, GREMI - STMicroelectronics, France, M. Boufnichel, STMicroelectronics, France, T. Tillocher, P. Lefaucheux, P. Ranson, R. Dussart, GREMI - Polytech Orleans/CNRS, France**

Gallium nitride (GaN) is currently used for light emitter devices due to a large and direct bandgap. Otherwise, GaN physical properties open new prospects in microelectronics manufacturing. By combining a wide bandgap (3.4 eV), strong chemical bonds and a high electron mobility, GaN based devices should operate under higher temperature, higher power and higher frequency than typical silicon devices.

It was shown that wet etching is limited due to inert chemical nature of GaN [1], especially in the c-plan where the etching is generally needed [2]. Therefore, plasma etching is essentially used due to the combination of chemical and physical effects. Chlorine plasmas are used because GaCl₃ is the most volatile Ga etching product.

Due to the power density applied to the next generation of power devices, an etched depth as high as 6 to 10 μ m is typically required. This could be qualified as deep GaN etching compared to the etched depth needed for light emitter devices which are of the order of few hundreds nanometers.

It was shown that bottom surface defects are linked with dislocations and nanopipes created during the epitaxial growth of GaN [3]. We will show that etched surface presents either pits or columnar defects closely linked with plasma conditions. Mass spectrometry data confirms the importance of CIO species in columnar regimes. We will show that SiCl₄ is able to scavenge CIO and allows to provide a smoother surface. SiCl₄ can be added in plasma gas or as the etching product of a silicon coverplate. We will also present data showing the influence of SiCl_x passivation layer on SiO₂ hard mask selectivity. Plasma diagnoscics such as optical emission spectroscopy or mass spectrometry will allow us to propose mechanism of formation of this passivation layer.

[1] D. Zhuang and J.H. Edgar, Mat. Sci. and Eng., 48 (2005) 1-46

[2] D. A. Stocker, E. F. Schubert, and J. M. Redwing. Applied Physics Letters, 73 (1998) 2654–2656

[3] J. Ladroue, A. Meritan, M. Boufnichel, P. Lefaucheux, P. Ranson, and R. Dussart, J. Vac. Sci. Technol. A 28, (2010) 1226

9:20am PS1-ThM5 Etching Reaction Analysis of CoFeB by Carbon Monoxide / Methyl Alcohol Based Plasmas, K. Karahashi, T. Ito, S. Hamaguchi, Osaka University, Japan

Magneticrandom access memory (MRAM)devices, which are composed of magnetic-tunnel-junction (MTJ) stacks, have potential to replace static random access memory, dynamic access memory, and flash memory devices because they can provide high speed operation, low operating voltage, and nonvolatile storage. For the realization of high-density MRAM devices, dry etching of magnetic thin films must be developed. Argon ion milling seems to be almost the only etching technique available in the current manufacturing processes for MRAM devices. However, capabilities of Argonion milling for anisotropic and selective etching of magnetic films are severely limited and therefore new technologies of reactive ion etching (RIE) for magnetic films are now seriously sought.RIE processes based on CO/NH3 and CH3OH are candidates for selective etching processes of magnetic thin films. In this study, we have focused on etching processes of CoFeB alloy thin films and examined etching reactionscaused by energetic CO+ or O+ ions, which are considered to be the major etchants of CO/NH3 or CH3OH plasmas. We have determined the etching yields and analyzed surface reactions, using a mass-selected ion beam system. The ion beam system is designed to inject mono-energetic single-species ions into a sample surface in ultra-high vacuum conditions. The reaction chamber is equipped with an X-ray photoelectron spectroscopy (XPS) for in-situ chemical analyses of irradiated surfaces. The ion beam energy used in this study is in the range of 300-1000eV. The etching rates are determined from measured depth profiles of irradiated surfaces and ion fluxes. It has been found that the etching rates of CoFeB by Ar+ ions are smaller than those of CoFe. Therefore physical sputtering yields of such magnetic thin films are affected byboron atoms contained in them. The etching rates of CoFeB by CO+ ions are found to belower than those by Ar+and increasewiththe cobalt content. From XPS analysis of CO+ irradiated CoFeB surfaces, it has been found that, although cobalt does not oxidize, iron of CoFeBoxidizes and inhibits the etching reactions. Therefore, the etching rates of CoFeB by CO+ irradiation are dependent on the atomic compositions of CoFeB films. The results suggest that design of the atomic composition of CoFeBfilms is important also for the etching process development. This work was supported by the Semiconductor Technology Academic Research Center (STARC).

9:40am PS1-ThM6 The Etching Characteristics of Flexible Substrate in Inductively Coupled Plasma System for Flexible Electronics, Y.S. Chun, Y.H. Joo, C.I. Kim, Chung-Ang University, Republic of Korea

Recently, many attention was given to the flexible electronics due to its future applications, such as flexible display and e-paper, etc. In order to fabricate the devices on the flexible substrate, such as PES, PAR, and PI, the etching characteristics of the substrate should be studied respect to other deposited thin film layers because the surface roughness and etch by-products could affect the device performance. Also, the devices can be embedded in the flexible substrate, where the flexible substrate should be etched away.

In this study, polyarylate (PAR) and polyethersulfone (PES) flexible substrates were etched by using inductively coupled plasma (ICP) system at room temperature. BCl₃, CF₄, and Ar mixed chemistry gases were used to achieve a high etch rate and good selectivity respect to the other metal (Al) or oxide (ZnO) layers. The etching charactersits of the flexible substrate were studied by varying the process parameters, including process pressure, DC bias voltage, RF power, and gas mixing ratio. In addition to the etch rate and selectivity, the surface chemical bonding structure and roughness were studied because they are the important factors for the device fabrication and performance.

The etch rate and selectivty were measured by using a depth profiler (alphastep 500, KLA tencor) and the surface roughness was measured by atomic force microscopy (AFM). The chemical states of etched surfaces were investigated with X-ray photoelectron spectroscopy (XPS). The elemental analysis of etched surfaces was investigated with the auger electron spectroscopy (AES) analysis.

10:40am PS1-ThM9 Plasma Process Developments for Spintronics Devices, K. Kinoshita, Tohoku University, Japan INVITED

Demands for zero-standby-power systems have increased in order to realize low-carbon society. For this purpose, non-volatile spintronics devices which use magnetic tunnel junction (MTJ) are receiving much attention due to its endurance and high speed. Another important advantage of the spintronics devices is their compatibility to CMOS process. Up to now, 16 Mb MRAM has been in the market. And, developments are ongoing on 300 mm wafer of 90 nm CMOS node or beyond targeting Gb class memory capacity. To combine with the BEOL process, low temperature (<350 degree C) processes are required for additional processes to fabricate the MTJ cell. Use of plasma which enables low temperature process matches the needs.

Whether the target is memory or logic, following three plasma processes are the key to realize the spintronics devices: (a) Damage-less PVD of thin-film multilayered-stack materials. (b) Dry etch for magnetic multilayer stack materials. (c) Protective film CVD over MTJ cell. Multi-target magnetron PVD is the key equipment to deposit uniform, ultra-thin, multi-stacked MTJ. MgO barrier film quality determined the performances of the MTJ [1]. An Ar milling process has long been used to etch magnetic materials. C-O(X)-based chemistry is increasing attracting attention recently due to its high etch selectivity between hard mask Ta and magnetic materials [2]. Here, degradation of device performances by chemical modification of magnetic materials is one of the issues. Recovery treatment becomes important for the next step [3, 4]. Process chemistry of the protective film CVD should not degrade materials used in MTJ. In addition, high enough quality is needed to protect the MTJ cell during the following BEOL processes [5].

All the unit processes should be evaluated by the MTJ performances after fabricating MTJ in a BEOL structure. In addition, total coordination of BEOL process including these MTJ fabrication processes is required.

This work was supported by JSPS through its FIRST Program.

 K. Ono et al., Jpn. J. Appl. Phys. <u>50</u>, 023001 (2011). [2] I. Nakatani, IEEE Trans. Magn. <u>32</u>, 4448 (1996). [3] K. Kinoshita et al., Jpn. J. Appl. Phys. <u>49</u>, 08JB02 (2010). [4] K. Kinoshita et al., to be published on Jpn. J. Appl. Phys. <u>51</u>, (2012). [5] K. Suemitsu et al., Jpn. J. Appl. Phys. <u>47</u>, 2714 (2008).

11:20am **PS1-ThM11** Predictions of the Etch Behavior of Complex Oxide Films for High-k and Multiferroic Applications, *N. Marchack, J. Chen, J.P. Chang*, University of California at Los Angeles

The ongoing quest to improve the performance of integrated circuit devices has led to a burgeoning body of research in synthesizing multifunctional materials. However, these materials are often intrinsically etch resistant and thus ensuring high-fidelity patterning via plasma etching faces significant challenges. This study aims to demonstrate predictive capability for the etch behavior of novel materials, e.g. complex oxides, by combining an established phenomenological model with thermodynamics-based volatility diagram analysis. The material systems studied were the potential high-k dielectric HfxLayOz, and the multiferroic candidates YxMnyOz and BixFeyOz.

Experiments to validate the theoretical analysis were conducted an inductively coupled plasma (ICP) reactor equipped with a quadrupole mass spectrometer (QMS) for analyzing etch products and a quartz crystal microbalance (QCM) for measuring the etch rate *in situ*. The use of the QCM eliminated the need to subject the samples to unwanted reactions in atmosphere prior to etch rate measurement, and also allowed for materials that were unable to be analyzed by other methods such as spectroscopic ellipsometry. The reactor was also connected to a UHV transfer tube which allowed the surface composition to be studied via x-ray photoelectron spectroscopy (XPS) without exposure to ambient conditions.

The calculated etch rates of the HfxLayOz films in a 400W, 5 mT, Cl2 plasma varied from 8.3 to 181.9 Å/min (for -25V to -200V bias voltage, respectively), generally lower than that of pure HfO2etched in comparable conditions by ~16 to 31%. The maximum etch rate observed for a 400W, 15mT BCl3condition was 61 Å/min (at -175V), with net deposition (1.34 – 4.71 Å/min) observed below -75V bias voltage. QMS was used to characterize the etch products, with LaCl, LaO3, LaOCl and LaO2Cl (3.4 : 4.0 : 3.1 : 1.0) and LaB, LaB2O, LaBOCl and LaO2Cl (1.2 : 1.1 : 1.3 : 1.0) observed as the dominant La-containing species in Cl2 and BCl3conditions respectively. The surface compositions of the films post-etching revealed a decrease in the La and Hf fractions after Cl2 and BCl3exposure, with a more significant reduction in La compared Hf (~50% v. ~19%) as

determined via XPS. Similar analysis for the multiferroic oxides will be presented and comparative etch behavior analyzed through the aforementioned theoretical framework.

11:40am PS1-ThM12 Sub-30nm Pitch Patterning of FEOL Materials for Aggressively Scaled CMOS Devices for 10 nm Node and Beyond, H. Miyazoe, S. Engelmann, H. Tsai, M. Brink, B.N. To, IBM T.J. Watson Research Center, J. Cheng, C. Liu, IBM Research - Almaden, W.S. Graham, E.M. Sikorski, M.A. Guillorn, N.C.M. Fuller, E.A. Joseph, IBM T.J. Watson Research Center

As the feature size in CMOS technology continues to shrink, patterning below 40 nm pitch faces many challenges. Continued delays in production worthy EUV lithography has driven an interest in directed self-assembly (DSA) [1] and sidewall image transfer (SIT) [2] patterning. Both techniques can augment conventional lithographic patterning by providing sublithographic multiplication of feature pitch. In this work, we leverage the results of a parametric study of factors impacting fine feature patterning [3] to further optimize DSA and SIT based patterning in the sub 30 nm pitch regime. Recently, we successfully demonstrated the transfer of "fingerprint" DSA patterns to the materials typically used in front end of line (FEOL) processing. Patterning of Si, SiNx and SiOx at a ${\sim}28$ nm feature pitch using poly(styrene-block-methyl methacrylate) (PS-b-PMMA) block copolymers was shown [4]. In this work, we discuss further optimization of the etch processes used to pattern the organic underlayer in the masking material stack as well as the substrate material. The use of templated DSA to generate line-space structures in the aforementioned materials was used to investigate the control of critical dimension (CD), line edge roughness and line width roughness throughout the patterning process. SIT-based patterning using metal oxide or nitride films as the side-wall hard mask was used to generate patterns in FEOL materials down to ~25 nm pitch. Typically, the CD of end lines are larger than the target CD of nested lines in structures generated by SIT. Dense/iso loading-like effects and other mechanisms to explain this phenomenon are explored. These initial patterning studies may play an important role in understanding feature formation and density limiting ground rules in future technology nodes. This work is sponsored by the DARPA GRATE (Gratings of Regular Arrays and Trim Exposures) program under Air Force Research Laboratory (AFRL) contract FA8650-10-C-7038.

[1] J. Cheng *et al.*, SPIE 2010. [2] H. Yaegashi *et al.*, SPIE 2012. [3] H. Miyazoe *et al.*, AVS2011. [4] S. Engelmann *et al.*, SPIE 2012.

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