Plasma Science and Technology
Room: 25 - Session PS-MoM

Advanced FEOL/Gate Etching 1
Moderator: L. Diao, Mattson Technology

8:20am **PS-MoM1 Selective Etching of Spacer with Pulsing in Inductively Coupled Plasmas for FinFET Devices**, *B. Zhou, M. Titus, P. Friddle, M. Robson,* ***G. Upadhyaya****, G. Kamarthy,* Lam Research Corp*, S. Kanakasabapathy, E. Franke*, IBM Corp

The transition to 14 nm technology node has introduced an architectural shift from traditional planar devices to complex three-dimensional FinFET structures. A primary etch challenge for making FinFET devices is that of spacer etch wherein the topography of the FinFET devices requires the fin surface (Si) to withstand substantial over-etch in order to remove the spacer on the fin sidewalls. Typical targets for this etch comprises of < 1nm Si recess, good spacer profile fidelity, complete spacer removal on fin sidewalls and < 2nm spacer CD loss. With conventional etch methodologies, the process window for achieving these targets is narrow due to competing deposition and etch species that simultaneously co-exist in the plasma. Simply lowering the electron temperature or lowering the ion energy is not a solution since there is a tradeoff between spacer CD loss and Si recess. In this presentation, we will demonstrate that by using pulsing, the deposition and etch phases can be separated thereby yielding a wide process window and breaking the tradeoff to enable FinFET spacer etch. Various pulsing schemes will be contrasted with conventional continuous mode operation along with a discussion of the compatibility of the pulsed spacer process with downstream integration.

8:40am **PS-MoM2 Evaluation of Novel Spacer Etch Processes using a New Gas**, ***S. Engelmann****, E.A. Joseph, N.C.M. Fuller, W.S. Graham, E.M. Sikorski,* IBM T.J. Watson Research Center*, M. Nakamura, G. Matsuura,* Zeon Chemicals L.P.*, H. Matsumoto, A. Itou, T. Suzuki*, Zeon Corporation

The spacer etch process is a very critical element in the CMOS device process flow as it ensures and enables the electrical isolation of Source/Drain and Gate regions. We observed that during conventional spacer processes, very little difference in plasma polymer deposition onto the respective substrates could be noted. [1] A successful Nitride Spacer process was rather facilitated by a silicon etch process that was selective to oxide, where excess oxidation lead to a conversion of Silicon to Silicon oxide. This also means that the etch rates of the Nitride are limited by the simultaneous oxidation of the nitride. A potential solution to overcome this limitation would be to control the etch rate by polymer thickness, similar to high selectivity oxide etching. An evaluation of this approach has yielded similar results as the general etch mechanism proposed by Standaert et al. [2] A novel etch chemistry was also evaluated that enables a different etch mechanism that cannot be described by the general model.

The impact of this novel mechanism on spacer etch processes was evaluated for both, capacitive and inductive discharges. We furthermore evaluated the impact of this novel process on planar and non-planar device structures. The novel gas chemistry has also been evaluated to enable an oxygen free spacer process. We found that the lateral spacer loss can be eliminated and that Si loss can be effectively reduced by employing the novel process. The SiN footing can be effectively reduced by fine-tuning the ion/neutral ratio of the plasma discharge. The best results to date from a PDSOI 22nm testsite have yielded an SOI loss of about 2nm which is able to maintain all SiN on the gate sidewall while keeping the HM loss to about 4nm and reducing the SiN foot to less than 3nm.

[1] S. Engelmann et al., AVS 58th Int. Symp. & Exhibit. (2011)

[2] M. Schaepkens et al., J. Vac. Sci. Technol. A 17, 26 (1999)

9:00am **PS-MoM3 Anisotropic and Selective Etching of Novel Multifunctional Materials**, ***J.P. Chang***, University of California, Los Angeles **INVITED**

The introduction of new and improved materials into silicon based integrated circuits is a major contributor in the recent decade to enable the scaling of circuit density and performance in analog, logic, and memory devices. Many new materials, such as complex metal oxides, magnetic materials and phase change materials, are much harder to pattern, thus pose significant challenges to the design and selection of plasma etching chemistries. This talk focuses on understanding the plasma-surface interaction and reaction kinetics, offers an unique approach in that thermodynamics analysis guides the selection of gas-phase chemistry, and establishes a kinetics-based model containing salient attributes of the etch process. The significant gain deriving from this unique approach is the ability to assess a large array of materials, which possess different properties that dictates a careful balance between etch anisotropy and selectivity. Both theoretical and experimental results from recent research will be discussed using complex metal oxides and magnetic materials are model systems.

9:40am **PS-MoM5 High Selective Etching of SiN Based Material Over Si and SiO_2 using Evanescent Microwave Plasma for FINFET Spacer Applications**, ***A. Raley****, A. Ranjan, H. Kintaka, B. Messer, T. Mori, K. Kumar, P. Biolsi,* Tokyo Electron Technology Center, America, LLC*, A. Inada,* Renesas Electronics*, R. Jung, S. Kanakasabapathy*, International Business Machines – Research Group

For smaller than 22nm technology node devices, a FinFET (3-D) gate structure is needed to reduce gate leakage, decrease power consumption, increase drive current and control short channel effects. FinFET gate spacer etching presents challenges for conventional RIE process, since it requires highly anisotropic and selective etching of Silicon Nitride over Si/SiO2. Microwave power was delivered through radial line slot antenna generating high density evanescent microwave plasma. High density evanescent microwave plasmawith low self-bias at the wafer enables a highly selective and anisotropic etching of spacer. The bulk electron energy distribution determines the gas phase reaction rates that generate various radicals and ionic species. The etchant, passivant and ion flux to the wafer can be controlled by the energy distribution of Bulk electrons (T_e). T_e can be tuned in by adjusting the microwave power. High SiN selectivity over Si and SiO2 was achieved on blanket as well as patterned wafer using the evanescent microwave plasma etcher. In general, selectivity is achieved by controlling the polymer layer difference over SiN/Si/SiO2. The difference of pattern wafer/blanket wafer etch rates/selectivities can be explained by differences in transport of by ions and radicals through high aspect ratio features. The effects of loading of SiN, Si and resist materials on etch rates and selectivity will be reviewed.

This work was performed by the Research and Development team at TEL Technology Center America in joint development with IBM Research Alliance Teams in Albany, NY 12222. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities

10:00am **PS-MoM6 Highly Selective and Controllable Si_3N_4 Etching to Si and SiO_2 for sub-22-nm Gate Spacer using CF_3 Neutral Beam with O_2 and H_2**, ***D. Nakayama****, A. Wada, T. Kubota,* Tohoku University, Japan*, M. Haass, R.L. Bruce, R.M. Martin, N.C.M. Fuller,* IBM TJ Watson Research Center*, S. Samukawa*, Tohoku University, Japan

Silicon nitride is used as a gate sidewall spacer for aggressively scaled complementary metal-oxide-semiconductor (CMOS) devices because of their high thermal stability and excellent insulating property. Therefore, silicon nitride (Si_3N_4) etching (patterning) is one of the critical processes in sub-22-nm-CMOS device fabrication. During the patterning of the silicon nitride spacer film, damage to the Si surface typically occurs, resulting in silicon (Si) and Si dioxide (SiO_2) recess in the source/drain and shallow trench isolation (STI) respective regions. Additionally, loss of spacer film close to the top of the gate structure can occur during the excessive “over etch” necessary to enable a manufacturable process. The advent of non-planar device geometries only exacerbates the aforementioned challenges. Hence, extremely high selectivity of silicon nitride to both Si and SiO_2 is extremely critical.

We developed an alternative etching process to solve these problems using a “damage-free” neutral beam (NB) etching process. A typical NB apparatus consists of plasma and process chambers that are separated by a carbon aperture. The carbon aperture can effectively neutralize the charged particles and eliminate irradiation of UV photons from plasma when the plasma passes through it. Therefore, etching can proceed without any UV-induced damage caused by charged particles or high-energy photons from the plasma.

In this study, we proposed neutral beam etching using a new gas chemistry of CF_3I in addition with oxygen (O_2) and hydrogen (H_2) gases for the sidewall spacer etching process. By using CF_3I, we can ensure that an energetic neutral beam comprised primarily of CF_3 is generated and, as such, becomes the main etching species for Si_3N_4,during the patterning process. Additionally, surface polymerization and surface oxidation on SiO_2 and poly-Si can be precisely controlled by addition of O_2 and H_2 gases,

respectively. As a result, moderately high selectivity of Si_3N_4 to both of Si (6.2:1) and SiO_2 (18.6:1) could be achieved by optimizing the ratio of $CF_3I/O_2/H_2$. Additionally, on relaxed ground rule structures at ~ 240nm pitch and gate CD (L_{gate}) ~ 40nm, an optimized NB etching condition achieves complete removal of the spacer from the gate sidewall with negligible spacer loss at the top of the gate structure and < 2 nm SOI loss. These results demonstrate the potential of silicon nitride etching process using neutral beams for fabricating sub-22-nm gate sidewall spacers.

10:40am **PS-MoM8 Highly Selective Etching of Titanium Nitride Over Tantalum Nitride in Inductively Coupled Plasma**, ***W. Zhu***, *H. Shin, S. Sridhar, L. Liu, V.M. Donnelly, D.J. Economou,* University of Houston, *C. Lenox, T. Lii*, Texas Instruments

The etching properties of metal nitrides (TiN, TaN) for high-k metal-gate integration were investigated in a Faraday-shielded inductively coupled plasma. The effect of operating conditions such as pressure, bias, and gas composition in HCl/He plasmas were explored for isotropic, highly selective etching of TiN over TaN. High selectivity is required for advanced device architectures incorporating metal gates integrated with high-k gate dielectrics and etch-stop layers. Etch rates were obtained separately for TiN and TaN blanket films on Si using end-point detection (by monitoring the Si 288nm emission signal) and reflectance measurements using a He-Ne laser, verified by post-etching TEM cross-sectional profiles. The etching rates were measured to be 130±20 and 60±10 nm/min for TiN and TaN, respectively, using 30% HCl/He chemistry at 70mTorr and 400W in continuous wave plasma with no bias on the substrate. The higher etching rate of TiN compared to that of TaN can be attributed to the lower binding energy of TiN and higher volatility of $TiCl_4$ etch byproducts. The etching selectivity was 2:1 (TiN:TaN) under the condition investigated. Higher selectivity between TiN and TaN was achieved by adding trace amounts of O_2 (O_2 partial pressure $<1x10^{-4}$Torr): for very small oxygen additions, the etching rate of TiN remained unchanged, whereas that of TaN decreased significantly. At high enough additions of O_2, etching of both TiN and TaN was completely suppressed. A narrow window of selectivity was found by varying O_2 partial pressure. The film surface was characterized after etching using X-ray photoelectron spectroscopy (XPS). Cl_2/He plasmas were also studied and their similarities and differences with HCl/He plasmas will be discussed.

Work supported by Texas Instruments.

11:20am **PS-MoM10 Detailed Analysis of Si Substrate Damage Induced by HBr/O_2- and H_2-Plasma Etching and the Recovery Process Designs**, *Y. Nakakubo, A. Matsuda,* Kyoto University, Japan, *M. Fukasawa,* Sony Corporation, Japan, *Y. Takao,* Kyoto University, Japan, *T. Tatsumi,* Sony Corporation, Japan, ***K. Eriguchi***, *K. Ono*, Kyoto University, Japan

Hydrogen-containing plasmas have been widely used for fabricating Si-based electronic devices such as metal–oxide–semiconductor field-effect transistor (MOSFET). Plasma-induced Si substrate damage during shallow trench isolation and gate electrode formation processes has become one of the critical issues because the damaged structure is believed to not only degrade the electric performance but also enhance the parameter variations resulting in yield loss in mass production [1]. Due to its light mass, a hydrogen atom from plasma can penetrate deeper in Si substrate, and, consequently, forms the thicker damaged layer leading to the larger amount of Si loss in the source /drain extension region of MOSFET called “Si recess” [2]. Although the recovery mechanism of Si damage has been extensively studied, there have been few comprehensive process-design guidelines by taking into account the electrical characteristic degradation. In this study, we report detailed analyses of Si-damage recovery dynamics using a capacitance–voltage (C–V) technique, and provide respective recovery process guidelines for HBr/O2- and H2-plasma cases. Silicon wafers with thermal-oxide layer (2 nm) were damaged by HBr/O2-and H2-plasma treatments. Various annealing processes in N2 ambient with different “thermal budgets” were employed to address the impacts of the temperature and budget on the damage recovery. An SiO2-Capping layer was formed on some samples to simulate structural constraints in present-day MOSFET processes. Using the quantitative C–V technique (1/C2-based analysis), we found that, although HBr/O2-plasma induced a larger amount of Si damage (defect site), wet-etch stripping process was more effective due to thinner damaged layer thickness, further, the annealing process with temperatures higher than 850 ºC was found to be able to cure the structural defects. As for H2-plasma cases, on the other, the wet-etch was “insufficient” to remove the defects, resulting in a high conductive layer. Moreover, we observed that the annealing temperature (> 1050 ºC) rather than the budget was a primal parameter to cure the damage. The obtained results may be explained by “the defect-density or structural-constraint effect”. The present findings imply an important and useful guideline of the recovery process design of H-containing-plasma damage in future advanced devices. [1] K. Eriguchi *et al.*: J. Vac. Sci. Technol. **A 29**, 041303 (2011).[2] M. Fukasawa *et al.*: J. Vac. Sci. Technol. **A 29**, 041301 (2011).

11:40am **PS-MoM11 Time-modulated Plasma Etching for Next Generation Devices**, ***S. Sriraman***, *Y. Wu, G. Kamarthy, C. Rusu, J. Holland, A. Paterson, V. Vahedi*, Lam Research

Plasma etching has facilitated the continuation of Moore's Law from >1µm to now less than 20 nm and is used to enable next-generation semiconductor device technology. While etching is used to compensate for incoming lithographic limitations as well as non-uniformities from up-stream processes, it also offers ways to counter fundamental limitations of pattern dependent etching and atomic-scale mixing. In this context, time-modulated plasma etching is the key to address challenges arising in critical etch applications for <20nm technology nodes.

This paper will aim to discuss some fundamental factors in consideration for time-modulated plasma etching in a Transformer Coupled Plasma (TCP™) chamber and its outcomes on representative process applications. Using a combination of experimental results, diagnostics, and modeling & simulation, the advantages of different types of time-modulated plasma and their ability to control basic plasma properties will be covered. The role and benefits of independently controlling ions and neutrals to overcome limitations in etching and their applicability to next generation device architectures will be discussed.

Authors Index

Bold page numbers indicate the presenter

— B —

Biolsi, P.: PS-MoM5, 1
Bruce, R.L.: PS-MoM6, 1

— C —

Chang, J.P.: PS-MoM3, **1**

— D —

Donnelly, V.M.: PS-MoM8, 2

— E —

Economou, D.J.: PS-MoM8, 2
Engelmann, S.: PS-MoM2, **1**
Eriguchi, K.: PS-MoM10, **2**

— F —

Franke, E.: PS-MoM1, 1
Friddle, P.: PS-MoM1, 1
Fukasawa, M.: PS-MoM10, 2
Fuller, N.C.M.: PS-MoM2, 1; PS-MoM6, 1

— G —

Graham, W.S.: PS-MoM2, 1

— H —

Haass, M.: PS-MoM6, 1
Holland, J.: PS-MoM11, 2

— I —

Inada, A.: PS-MoM5, 1
Itou, A.: PS-MoM2, 1

— J —

Joseph, E.A.: PS-MoM2, 1
Jung, R.: PS-MoM5, 1

— K —

Kamarthy, G.: PS-MoM1, 1; PS-MoM11, 2
Kanakasabapathy, S.: PS-MoM1, 1; PS-MoM5, 1
Kintaka, H.: PS-MoM5, 1
Kubota, T.: PS-MoM6, 1
Kumar, K.: PS-MoM5, 1

— L —

Lenox, C.: PS-MoM8, 2
Lii, T.: PS-MoM8, 2
Liu, L.: PS-MoM8, 2

— M —

Martin, R.M.: PS-MoM6, 1
Matsuda, A.: PS-MoM10, 2
Matsumoto, H.: PS-MoM2, 1
Matsuura, G.: PS-MoM2, 1
Messer, B.: PS-MoM5, 1
Mori, T.: PS-MoM5, 1

— N —

Nakakubo, Y.: PS-MoM10, 2
Nakamura, M.: PS-MoM2, 1
Nakayama, D.: PS-MoM6, **1**

— O —

Ono, K.: PS-MoM10, 2

— P —

Paterson, A.: PS-MoM11, 2

— R —

Raley, A.: PS-MoM5, **1**
Ranjan, A.: PS-MoM5, 1
Robson, M.: PS-MoM1, 1
Rusu, C.: PS-MoM11, 2

— S —

Samukawa, S.: PS-MoM6, 1
Shin, H.: PS-MoM8, 2
Sikorski, E.M.: PS-MoM2, 1
Sridhar, S.: PS-MoM8, 2
Sriraman, S.: PS-MoM11, **2**
Suzuki, T.: PS-MoM2, 1

— T —

Takao, Y.: PS-MoM10, 2
Tatsumi, T.: PS-MoM10, 2
Titus, M.: PS-MoM1, 1

— U —

Upadhyaya, G.: PS-MoM1, **1**

— V —

Vahedi, V.: PS-MoM11, 2

— W —

Wada, A.: PS-MoM6, 1
Wu, Y.: PS-MoM11, 2

— Z —

Zhou, B.: PS-MoM1, 1
Zhu, W.: PS-MoM8, **2**