Graphene and Related Materials Focus Topic
Room: 13 - Session GR+EM+NS+PS+SS+TF-MoM

Graphene Growth

Moderator: M. Spencer, Cornell University, V.D. Wheeler, U.S. Naval Research Laboratory

8:20am **GR+EM+NS+PS+SS+TF-MoM1 Synthesis Ingredients Enabling Low Noise Epitaxial Graphene Applications**, ***D.K. Gaskill***, *L.O. Nyakiti, V.D. Wheeler,* U.S. Naval Research Lab, *A. Nath,* George Mason Univ., *V.K. Nagareddy,* Newcastle University, UK, *R.L. Myers-Ward, N.Y. Garces, S.C. Hernández, S.G. Walton,* U.S. Naval Research Lab, *M.V. Rao,* George Mason Univ., *A.B. Horsfall,* Newcastle Univ., UK, *C.R. Eddy, Jr.,* U.S. Naval Research Lab, *J.S. Moon*, HRL Labs LLC

Sensors made from graphene flakes have demonstrated single molecule detection [Schedin *et al*., Nat Mat **6**, 652 (2007)]; this ultra-sensitivity is likely due to the high crystalline quality of the graphene and the associated relative lack of defects that give rise to noise. The low noise nature of high quality graphene should also facilitate other applications, e.g., low-noise amplifiers. Combined with the unique ambipolar property of graphene field effect transistors (FETs), the low noise character of graphene would significantly advance the performance of frequency multipliers, mixers and high-speed radiometers. To exploit these applications, high quality, reproducible wafer-scale epitaxial graphene (EG) with minimal thickness variations and defects are essential requirements. Here, crucial graphene synthesis elements required to achieve the wafer-scale quality goal are described. Understanding the effect of substrate misorientation as well as hydrogen etch and Si sublimation conditions for graphene synthesis on the (0001) SiC surface is essential to achieve improved and reproducible wafer-scale graphene quality. For example, the impact of processing factors such as temperature control, laminar gas flow and substrate rotation on large area EG uniformity are described using examples created in an Aixtron SiC epitaxy reactor. In addition, managing SiC step formation on the nominal (0001) orientation is significant for achieving uniform EG thickness on terraces and to minimize additional growth at the step edges; this is illustrated using data from atomic force microscopy and scanning electron microscopy images in combination with Raman spectroscopy maps and x-ray photoelectron spectroscopy analysis. Managing step formation combined with optimal growth leads to the suppression of the Raman defect "D" band confirming minimal grain boundaries and defects, which are additional sources of electronic noise. Lastly, contactless Lehighton resistivity maps of 75 mm wafers are used to illustrate the overall uniformity of optimally synthesized graphene as well as to show the re-sistance state-of-the-art, with individual wafers exhibiting about a ±3% relative variation. Examples of the impact of this synthesis approach on chemical sensors devices and FETs will be shown, each exhibiting 1/f noise behavior down to 1 Hz and possessing noise spectral densities similar to reports from exfoliated graphene. Hence, careful control of EG formation across the wafer results in improved quality which subsequently leads to the reduction or elimination of additional noise sources from graphene defects that would then adversely affect device performance.

8:40am **GR+EM+NS+PS+SS+TF-MoM2 Growth of Graphene by Catalytic Decomposition of Ethylene on Cu(100) and Cu(111) With and Without Oxygen Predosing**, ***Z.R. Robinson***, *P. Tyagi, T. Mowll, C.A. Ventrice, Jr.,* University at Albany- SUNY, *K. Clark, A.-P. Li*, Oak Ridge National Laboratory

Graphene growth on Cu substrates has become one of the most promising techniques for the mass production of graphene, and therefore significant effort has been put into developing growth conditions that lead to large area, defect and grain boundary free graphene films. One key consideration is the influence that the underlying copper substrate has on the growth of the graphene. In order to study this, graphene growth on Cu(100) and Cu(111) was carried out in a UHV system. The samples were heated using an oxygen series button heater. The hydrocarbon pressure was measured using a capacitive manometer instead of an ion gauge, which could cause dissociation of the hydrocarbon molecules. Initially, it was found that annealing the crystals to 900 °C resulted in impurity segregation at the surface. Several cycles of sputtering at 600 °C were required to remove all bulk impurities so that the surface remained clean even after annealing to 900 °C. Initial attempts to grow graphene by annealing each crystal to temperatures as high as 900 °C in UHV, followed by backfilling the chamber with up to 5 x 10^{-3} torr of C_2H_4 did not result in graphene formation. It was found that by first backfilling the chamber with C_2H_4 and then raising the temperature from 25 °C to 800 °C, graphene growth could be achieved. A four-domain epitaxial overlayer is observed for the Cu(100) surface. Pre-dosing the Cu(100) with oxygen at 300 °C, which forms a saturation coverage of chemisorbed oxygen, was found to result in a 2-domain graphene overlayer using similar growth conditions. A study of the effect of oxygen pre-dosing on the growth of graphene on Cu(111) has been initiated.

9:00am **GR+EM+NS+PS+SS+TF-MoM3 Impact of Growth Parameters on Uniformity of Epitaxial Graphene**, ***L.O. Nyakiti***, *V.D. Wheeler, R.L. Myers-Ward, J.C. Culbertson,* U.S. Naval Research Laboratory, *A. Nath,* George Mason University, *N.Y. Garces,* U.S. Naval Research Laboratory, *J. Howe*, Oak Ridge National Laboratory, *C.R. Eddy, Jr., D.K. Gaskill*, U.S. Naval Research Laboratory

Epitaxial graphene (EG) offers a facile method for attaining large area graphene for device applications. Since wafer uniformity and thickness control is vital, a systematic study of the parameters affecting the EG growth process was performed and the optimal conditions for obtaining uniform morphology and high electronic quality were determined. EG was synthesized in a low pressure Ar flowing ambient on 8x8mm^2 6H-SiC(0001) substrates that were offcut 0.8^o from the basal plane, using an Aixtron VP508 reactor. The samples were placed on a rotating ~100 mm diameter susceptor and excellent EG layer uniformity and run-to-run reproducibility were obtained. The investigation focused upon the critical synthesis parameters of temperature (T) (1520-1660^{o}C) and time (t) (15-60 min), an *in-situ* H_2 etch conditions (1520-1600^{o}C for 10-30min). Morphology, layer thickness, chemical analysis, and strain variations across the samples were characterized using electron microscopy, AFM, XPS and μ-Raman spectroscopy. Large-area van der Pauw Hall effect was performed to quantify the graphene mobility (μ), and carrier density. Results show that growth T and t had the most significant impact on EG electronic and morphological properties. For example, synthesis at 1660^{o}C for 30min resulted in 4-8 monolayers (ML) and a step-bunched morphology with high concentration of wrinkles originating from the step-edge and pinned at the nearest terrace edge. Other morphological features were pits primarily located at the step edges having a depth ~20nm and density 6.4x10^6 cm^{-2}. In contrast, EG synthesis at 1520^{o}C for 30min results in uniform ML coverage along the terrace width that is devoid of pits and wrinkles. Mobility was found to have a drastic dependence on graphene thickness. Under optimal conditions, 1-2 ML were obtained and μ as high as 1240 cm^{2}V^{-1}s^{-1} was achieved; in contrast, for EG with >2 ML μ ~ 550 cm^{2}V^{-1}s^{-1}, presumably due to interlayer interaction and electronic screening. XPS C1s and Raman 2D spectra of EG grown on substrates after undergoing *in-situ* H_2 etch at different times did not show shifts in peak position/intensity suggesting lack of etch time dependence on EG electronic or structural quality. Yet etch conditions affect the final morphology, as EG synthesis performed after an *in-situ* H_2 etch at 1600^{o}C resulted in step-bunched morphology with step heights 5-10nm, whereas, substrates etched at 1520^{o}C had EG with step-heights 10-15nm. In addition other growth parameters investigated were found to be of secondary importance, including: Ar pressure, flow rates, and sample cool down conditions.

9:20am **GR+EM+NS+PS+SS+TF-MoM4 Uniform Epitaxial Growth of Charge Neutral Quasi-Free-Standing Monolayer Graphene on a 6H-SiC(0001) Surface by Combination of Metal Silicidation and Intercalation**, ***H. Shin***, *I. Song, C.-Y. Park, J.R. Ahn*, Sungkyunkwan University, Republic of Korea

Intrinsic high mobility of graphene are much reduced in graphene devices by various factors. Two critical factors degrading mobility are uniformity in an atomic structure such as number of a layer and an interaction with a substrate. Recently Shuai-Hua Ji *et al.* reported quantitatively that conductivity is much reduced by one sixth when electrons pass through a boundary between monolayer and bilayer graphene at a step edge in comparison to conductivity of monolayer graphene. This suggests that uniformity of number of graphene layer is a more crucial factor than expected. In particular, in epitaxial graphene on SiC, the uniformity of number of layer is an intrinsic and serious problem because Si is more rapidly sublimated near a step edge in the formation of epitaxial graphene by thermal evaporation of Si and, subsequently, epitaxial graphene with different layers coexists intrinsically on a terrace. Another factor degrading mobility is an interaction between graphene and a substrate. In epitaxial graphene, the interaction was reduced by intercalation of metal or molecule such as H, F, and Au between graphene and a substrate, which results in quasi freestanding graphene. Various charge neutral quasi freestanding graphene has been reported, but the charge neutrality was found at an optimal coverage of an intercalated element and annealing temperature. This makes it difficult to achieve spatially homogeneous charge neutrality of quasi freestanding graphene, and a method with a broad range of

coverage and temperature is demanded. We demonstrate that charge neutral quasi freestanding monolayer graphene can be grown uniformly without coexistence of a buffer layer and a bilayer graphene which limit mobility of epitaxial monolayer graphene. Because coexistence of two different phases is inevitable on a SiC surface, uniform monolayer graphene was produced based on two different phases, a Si-rich phase and a C-rich phase called a buffer. Pd was deposited on both the Si-rich and C-rich phases and annealed up to 900°C. The Si-rich phase produced Pd silicide and charge neural quasi freestanding monolay graphene was produced on the Pd silicide while, on the C-rich phase, Pd was intercalated between the buffer layer and SiC resulting in charge neutral quasi freestanding monolayer graphene, where the quasi freestanding monolayer graphene on two difference regions was connected atomically. The combination of Si silicidation and intercalation result in uniform charge neutral quasi freestanding uniform monolayer on a SiC surface, where the electronic and atomic structures were observed using angle-resolved photoemission spectroscopy and scanning tunneling microscopy.

9:40am **GR+EM+NS+PS+SS+TF-MoM5 Epitaxial Graphene on Ir(111) - A Playground for the Fabrication of Graphene Hybrid Materials**, ***T.W. Michely***, Universität zu Köln, Germany **INVITED**

Carefully optimizing the growth of graphene on Ir(111) yields a virtually defect free, weakly bound epitaxial monolayer ranging from quantum dot sizes to macroscopic extension. In the talk I will show how this system can be used to construct new types of graphene based materials. Specifically, patterned adsorption of transition metals results in dense cluster arrays with exciting magnetic and catalytic properties. Intercalation underneath the graphene allows one to manipulate the properties of graphene itself, e.g. its ability to adsorb atoms and molecules as well as its magnetism.

10:40am **GR+EM+NS+PS+SS+TF-MoM8 Graphene Growth Studied with LEEM, PEEM, EELS, ARPES, MEIS, and STM**, ***R.M. Tromp***, *J.B. Hannon, M.W. Copel, S.-H. Ji, F.M. Ross*, IBM T.J. Watson Research Center **INVITED**

We have studied the growth of graphene on a variety of substrates, including SiC (both Si and C terminated), polycrystalline Cu and Ni foils, as well as single-crystal Ni foils. Low Energy Electron Microscopy (LEEM) and Photo Electron Emission Microscopy (PEEM) offer the unique opportunity to follow the growth in real time, as it proceeds at high temperature, and in the presence of processing gases such as disilane (for growth on SiC) or ethylene (for growth on the metal substrates). Low Energy Electron Diffraction (LEED) allows us to determine crystallographic orientations as well as atomic structure of areas well below a micrometer in extent. Information on electronic structure can be obtained from the plasmon loss features using Electron Energy Loss Spectroscopy (EELS), or from Angle Resolved Photo Electron Spectroscopy (ARPES). These spectroscopic experiments are carried out in the LEEM/PEEM microscope using an in-line energy filter with which energy and angle resolved analysis of the electrons can be performed on selected areas. Finally, to obtain information on the layer-by-layer evolution of the graphene films, particularly on SiC, we have used isotope sensitive Medium Energy Ion Scattering (MEIS), to follow the growth by thermal decomposition of ^{12}C vs ^{13}C graphene monolayers from a three-bilayer thick $Si^{13}C$ homoepitaxial film grown on a SiC substrate. Taken together, these results provide a comprehensive view of the growth of graphene films. In this talk, we will review the most salient results of these studies, and their relevance to the use of graphene films for electronic applications. To address the latter, we will discuss the results of three-probe STM experiments in which we measured the excess resistivity of a graphene sheet as it crosses an atomic step of the underlying substrate.

11:20am **GR+EM+NS+PS+SS+TF-MoM10 Spatial Confinement of Epitaxy of Graphene on Microfabricated SiC to Suppress Thickness Variation**, ***H. Fukidome***, *T. Ide, H. Handa*, RIEC, Tohoku Univ., Japan, *Y. Kawai*, Tohoku Univ., Japan, *F. Fromm*, Univ. Erlange-Nürnberg, Germany, *M. Kotsugi, T. Ohkouchi*, JASRI/SPring-8, Japan, *H. Miyashita*, Tohoku Univ., Japan, *Y. Enta*, Hirosaki Univ., Japan, *T. Kinoshita*, JASRI/SPring-8, Japan, *Th. Seyller*, Univ. Erlange-Nürnberg, Germany, *M. Suemitsu*, RIEC, Tohoku Univ., Japan

Epitaxial graphene on SiC (EG) is promising owing to a capability to produce high-quality film on a wafer scale [1]. One of the remaining issues is microscopic thickness variation of EG near surface steps, which induces variations in its electronic properties and device characteristics. To suppress the variation, spatial confinement of surface reactions is effective. The spatial confinement using substrate microfabrication, for instance homoepitaxy and sublimation on microfabricated Si substrates, can induce self-ordering of steps, and even produce step-free surfaces [2]. The spatial confinement is therefore anticipated effective to obtain EG without the thickness variation.

We have for this reason applied the spatial confinement to the epitaxy of graphene on 6H-SiC(0001). For the spatial confinement, 6H-SiC(0001) substrates were microfabricated by using electron beam lithography and fast atomic beam etching using sulfur hexafluoride [3, 4]. Epitaxial graphene on the microfabricated 6H-SiC(0001) substrates was obtained by annealing at 1923 K in Ar ambience [2]. It is verified by using low energy electron microscopy (LEEM) and photoemission electron microscopy (PEEM) that step-free SiC surface and EG without thickness variation can be formed on smaller patterns [4]. This result clearly demonstrate that the spatially confinement is effective for the epitaxy of graphene on SiC. Furthermore, Raman spectroscopy and LEEM reveals that the spatial confinement can suppress the fluctuations of the electronic properties, e.g. (unintentional) doping in EG [4].

In conclusion, we have demonstrated that the spatial confinement of EG is effective to control both structural and electronic properties. This novel technique can boost the development of electronic devices based on EG.

[References]

[1] K. V. Emstev et al., Nature Mater. 8 (2009) 203.

[2] Y. Homma et al., Jpn. J. Appl. Phys. 35 (1996) L241.

[3] T. Ide et al., accepted for the publication in Jpn. J. Appl. Phys.

[4] H. Fukidome et al., submitted.

11:40am **GR+EM+NS+PS+SS+TF-MoM11 Three-Dimensional Graphene Architecture Growth and Its Facile Transfer to Three-Dimensional Substrates**, ***J.-H. Park***, Sungkyunkwan University, Republic of Korea, *H.-J. Shin, J.Y. Choi*, Samsung Advanced Institute of Technology, Republic of Korea, *J.R. Ahn*, Sungkyunkwan University, Republic of Korea

Recent development of large area graphene synthesis on metal layer by chemical vapor deposition (CVD) or epitaxial growth on silicon carbide (SiC) opened the possibility for applications such as transparent electrodes for ITO replacement. For instance, graphene has been demonstrated for use in a liquid crystal display (LCD) and/or organic light emitting diode (OLED) test cell as a bottom electrode. However, the actual device, e.g., an active-matrix (AM) LCD, operates by switching individual elements of a display, using a thin-film transistor (TFT) for each pixel. Here, the pixel electrode of a display should extend down to the transistor's source or drain, thereby making contact with a via hole, which demands that a three-dimensional (3D) architecture electrode be deposited on a flat surface as well as its side walls. Although large-area graphene growth can be applied for a wide range of applications, 3D graphene architecture growth has not been realized for actual devices due to the original limitation of planar graphene growth. Herein, we demonstrate for the first time 3D graphene architecture growth and its facile transfer to a planar and/or 3D substrate. To prevent agglomeration of nano-scale metal catalyst by the CVD process, we chose a SiC system. Graphene, a few layers thick, was epitaxially grown on a pre-patterned SiC substrate with nano-size thickness which was produced by photolithography and dry etching. Graphene on a vertical facet of the SiC pattern with a few-hundred nanometers in height was perfectly prepared using this approach, contrary to the CVD method. Furthermore, we suggest the use of a facile transfer method of graphene on SiC to a SiO2 substrate using thermal release tape after hydrogen intercalation. In spite of the troublesome transfer issue of SiC, the geometry of the 3D graphene was perfectly transferred onto the planar SiO2 as well as the 3D SiO2 structure. In other words, the 3D graphene architecture was maintained as a floating cap structure on planar SiO2 and the vertical facet of the 3D SiO2 structure was well covered. Moreover, the graphene bottom layer without a 3D cap and the inverted bowl structure in the 3D graphene architecture were selectivly transferred by controlling intercalation and pressure. These approaches could provide a beneficial method for preparing a 3D graphene architecture as well as for modifying the ordered structure to be utilized in real devices.

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