Graphene and Related Materials Focus Topic
Room: 13 - Session GR+AS+NS+SS-ThM

Graphene Nanostructures
Moderator: A. Kis, EPFL, Switzerland

8:00am **GR+AS+NS+SS-ThM1 Atomic and Electronic Structures of Graphene Nanoribbon made by MBE on Vicinal SiC Substrate**, ***F. Komori***, *K. Nakatsuji, T. Yoshimura,* University of Tokyo, Japan, *T. Kajiwara, K. Takagi, S. Tanaka*, Kyushu University, Japan

Electronic states of graphene nanoribbon attract much interest because its intrinsic metallic band is modified to have a gap or a one-dimensional edge state at the Dirac energy E_D. Actually, microfabricated graphene [1] showed an energy gap at E_D, and the gap size increases with decreasing the width. Fabrication of well-controlled graphene nanoribbons on macroscopic area of a semiconductor substrate is, however, still one of the challenging issues in graphene research. Here, we report characterizations of graphene nanoribbon made by carbon molecular beam epitaxy (MBE) and a hydrogen treatment on a vicinal SiC(0001) substrate. Use of MBE is essential because graphene is made over the step edges of the SiC substrate in the case of graphene formation by widely-used thermal decomposition.

In the experiment, a $6\sqrt{3}$ x $6\sqrt{3}$ structure was first made by MBE on the anisotropic terrace of the Si-terminated surface of a nitrogen-doped 6H-SiC(0001) substrate vicinal to the [1-100] direction. The tilting angle of the substrate was 4 degree, and a well-ordered step-and-terrace structure was made after cleaning the substrate by annealing in hydrogen as confirmed by atomic force microscopy. We optimized the substrate temperature and the carbon deposition rate to make a homogeneous $6\sqrt{3}$ x $6\sqrt{3}$ structure on the terraces without thermal decomposition of the substrate. The surface structure was *in situ* monitored by reflection high energy electron diffraction, and the width of the $6\sqrt{3}$ x $6\sqrt{3}$ area on the terrace was adjusted by monitoring the $6\sqrt{3}$ x $6\sqrt{3}$ spots. After stopping the growth, the sample was exposed to hydrogen molecules at 600 °C to transform the surface $6\sqrt{3}$ x $6\sqrt{3}$ layer to single-layer graphene by inserting hydrogen atoms at the interface. [2]

Graphene honeycomb lattice without the $6\sqrt{3}$ x $6\sqrt{3}$ structure was confirmed by low energy electron diffraction and scanning tunneling microscopy (STM). Few point defects are seen at the graphene on the terrace in the STM images of atomic resolution. The width of graphene nanoribbon on the substrate terrace is 10-15 nm, depending on the growth condition. The electronic states of the graphene nanoribbon were studied using angle-resolved photoemission spectroscopy (ARPES) at 130 K as in the previous report. [3] The top of the π band of the graphene nanoribbon was 0.05 ~ 0.25 eV below the Fermi energy. No signal from the π^* band was detected by ARPES above the top of the π band, indicating the gap formation at E_D.

References

1. M. Y. Han *et al*., Phys. Rev. Lett. **98**, 206805 (2007).

2. C. Riedl *et al*., Phys. Rev. Lett. **103**, 246804 (2009).

3. K. Nakatsuji *et al*., Phys. Rev. B**82** 045428 (2010).

8:20am **GR+AS+NS+SS-ThM2 Carrier Transport Behavior of Carbon Nanotube Transistors with Single Semiconducting and Metallic Tube**, *P. Sakalas,* ***M. Schroter***, Technische Universität Dresden, Germany

The high interest in using carbon nanotube FETs in advanced electronics is based on their unique 1D transport properties such as quasi-ballistic transport. The high carrier velocity together with the quasi 1D tube geometry yield a very low intrinsic capacitance per tube of approximately 80 aF/mm in multitube structures. Those properties makes CNTFETs very interesting for high frequency and power applications.

CNTFETs with a single semiconducting tube yield too low current (25 µA) for useful applications and thus the transistors with thousands tubes in parallel are being fabricated [1][2]. unfortunately, following theory 1/3rd of all tubes are metallic. Carrier scattering is better understood for metallic tubes and it is believed that for semiconducting tubes, despite more complexity, the same scattering mechanisms are applicable: CNTs defect scattering, physical bends and phonon scattering are present. Investigation of CNTFETs with a single semicoducting (ST), single metallic (MT) and metallic+semiconducting (MST) tubes at different lattice temperature environment was never done before and enables a deeper insight of CNT transport properties to further improve the application-oriented device behavior. It was shown that multifinger CNTFETs exhibited a weak temperature dependence of IV, RF and NF indicating a very weak electron-phonon interaction and the absence of charge-carrier freeze-out known for conventional doped semiconductors [3],[4].

In this work transistors with single ST, single MT and double MST were selected. Transistors have 800 nm channel length and features n-type behavior. IV characteristics were measured on wafer for manufacturable CNTFET process selected single CNTs at different lattice temperatures. The investigated structures have a fixed gate length of 0.35 µm and gate width of 40 µm. The source-drain spacing (channel length) is 800 nm. A 20 nm thick HfO2 was used for the gate oxide. The devices were fabricated with the process technology described in [1][2].The CNTFETs were embedded in DC pads for on-wafer measurements. Transfer characteristics of ST and MT transistor structures at ambient temperature T0 = 300 K, are shown in Fig.1 and Fig.2, Fig.3, Fig.4. The drain current show saturation for ST device, typical for MOSFETs. Nevertheless the carrier transport is very different. The dependence of drain current over the temperature will enable the analysis of transport behavior of single ST and MT and coupled MST. As it is seen from Fig.3 and Fig.4 the MT transistor structure behaves as nonlinear resistor.

8:40am **GR+AS+NS+SS-ThM3 Fabrication of Chemically–isolated Graphene Nanoribbons (GNRs) by Scanning Probe Nanolithography using a Heated Probe**, ***W.K. Lee***, *J.T. Robinson, R. Stine, C.R. Tamanaha, D. Gunlycke,* Naval Research Laboratory, *M. Haydell, E. Cimpoiasu,* U.S. Naval Academy, *W. King,* University of Illinois at Urbana Champaign, *P.E. Sheehan*, Naval Research Laboratory

One route to realizing graphene as a material for digital-type devices is through the lithographic patterning of graphene nanoribbons (GNRs). GNRs enable band gap engineering that is dependent on nanoribbon width and edge state. We employed two complementary AFM-based lithography techniques to pattern GNRs: (1) thermal dip-pen nanolithography (tDPN)[1] and (2) thermochemical nanolithography (TCNL)[2]. Though inverse in approach, both techniques generate GNRs into a larger sheet of insulating chemically-modified graphene. Both lithographies were performed on CVD-grown single-layered graphene (SLG) on SiO_2/Si substrates using heated AFM probes. The first approach, tDPN, used the heated probe to deposit narrow polystyrene (PS) ribbons on pristine graphene. The areas of the graphene not protected by the polymer were then fluorinated, converting them to a highly insulating state, which leaves behind a chemically isolate GNR channel. We show that the PS protected ribbon was the only conductive pathway for active device. Secondly, we use the converse approach by using the heated AFM probe to locally reduce fluorographene back to graphene, leaving behind a conductive GNR channel. Both techniques can generate a wide range of nanoribbon widths while avoiding electron beams which can damage graphene. We discuss the relative merits of each strategy, as well as their impact on electrical properties (e.g., doping).

1. WK Lee et al., *Nano Letters*, 11, 5461, 2011

2. Z Wei et al., *Science*, 328, 1371, 2010

9:20am **GR+AS+NS+SS-ThM5 Growth of a Linear Topological Defect in Graphene as a Gate-tunable Valley Valve**, ***A. Zettl***, *J.-H. Chen, N. Alem,* Univ. of California at Berkeley, Lawrence Berkeley Lab, *G. Autes, F. Gargiulo,* Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, *A. Gautam, M. Linck,* Lawrence Berkeley National Lab, *C. Kisielowski,* Lawrence Livermore National Lab, *O.V. Yazyev,* Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, *S.G. Louie*, Univ. of California at Berkeley, Lawrence Berkeley Lab **INVITED**

The valleytronics, a zero-magnetic-field equivalent of spintronics, could be realized in graphene if a simple scheme can be conceived to generate and to detect valley polarization in the material. Here we provide the first direct experimental observation of the self-sustained, atomically controlled growth of a peculiar linear defect structure in suspended graphene. The structure consists in units of octagon and pentagon pairs (termed 5-5-8 defect) and can be grown from a single pentagon seed in graphene under electrical bias. First-principle simulations show that the 5-5-8 defect can act as a gate-tunable valley valve. The result represents a critical step towards realizing valleytronics in graphene.

10:40am **GR+AS+NS+SS-ThM9 Crystalline and Electrical Properties of Vertically-Laminated Carbon Nanowalls formed by Two-Step Growth Method**, ***H. Kondo***, *T. Kanda,* Nagoya University, Japan, *M. Hiramatsu,* Meijo University, Japan, *K. Ishikawa, M. Sekine, M. Hori*, Nagoya University, Japan

Carbon nanowall (CNW) is one of carbon nanomaterials consisting of stacked graphene sheets, which are vertically standing on the substrate. Due to the unique properties of graphene sheets, such as high carrier mobility,

large current carrying capability, and so forth, it is expected that the CNW also have such the excellent electrical and physical properties. On the other hand, In the CNWs, the bending and branching graphene sheets take a maze-like form. Therefore, due to their unique morphology and properties, the CNWs are promising as channel and electrode materials in the various types of the future nanoelectrics devices. At the construction of the CNW devices, vertical lamination of different types of CNWs is one of the useful and important technique as basic elements of the devices.

In this study, we investigated sequential two-step growth of CNWs to form the vetically-laminated structures. In this experiment, two types of CNW growth processes with different conditions were sequentially performed on Si substrate by an electron beam excited plasma-enhanced chemical vapor deposition (EBEP-CVD) using CH4/H2 mixture gas. Firstly, the CNW was grown at 600°C and 2.67 Pa for 10 min. Then, the second-step growth process was performed at 480°C for 10 min. The CNW samples formed only by the single-step growth at 480°C or 600°C were also prepared for comparison. Morphology and crystalline structures of CNWs were analyzed by scanning electron microscopy and Raman spectroscopy.

In the case of the single-step growth, only after the growth at 600°C, about 600 nm-thick CNWs were formed, although CNWs hardly grew at 480°C. On the other hand, in the case of the step-growth, about 1200 nm-thick CNWs were formed after the second-step growth at 480°C, compared to the single-step growth at 600°C. No boundary was found between the lower and upper region. The stacks of graphene sheets formed seamless structures. According to the Raman spectra, the crystalline structures of the CNWs were hardly changed even after the first-step growth at 600°C and the second-step growth at 480°C. This result means that the nanographene can restart to grow easily and continuously at the edges of the previously-grown graphene even at 480°C without the nucleation. These results indicate the possibility to realize the vertical junction of different types of CNWs, such as a p-n junction. At the session, the interfacial structures and electrical properties of the vertically-laminated CNWs will also be discussed.

11:00am **GR+AS+NS+SS-ThM10 Surface Modification of Vertically Oriented Graphene Electrochemical Double-Layer Capacitors**, ***R.A. Quinlan***, Naval Surface Warfare Center, Carderock Division, *M. Cai,* The College of William and Mary, *A.N. Mansour,* Naval Surface Warfare Center, Cardercock Division, *R.A. Outlaw*, The College of William and Mary

Previously reported efforts have identified the potential of vertically oriented graphene nanosheets in electrochemical double-layer capacitors (Miller et. al, Science 2010) for efficient AC line-filtering performance. Continued investigations to improve performance suggest that the availability of a high edge and surface defect density could be the dominant mechanism. Furthermore, charge/discharge profiles over time show that performance can actually increase as the device ages. In an effort to understand these findings, X-ray photoelectron spectroscopy, Auger electron spectroscopy and near edge absorption fine structure spectroscopy have been utilized to study the interaction of the electrolytes and solvents with the graphene-based electrode materials. The EDL capacitance of graphene nanosheets has been measured before and after Ar plasma bombardment for various times and after exposure to water, isopropanol, methanol, NaOH and KOH. Graphene nanosheet electrochemical capacitors have been disassembled and analyzed following short term and long term operation.

11:20am **GR+AS+NS+SS-ThM11 Electronic Properties and Device Applications of Wafer-Scale Graphene Nanoribbons**, ***D. Jena***, University of Notre Dame **INVITED**

Graphene boasts unique physical, electronic, and optical properties. For conventional electronic device applications, the zero band gap of 2-dimensional graphene is an impediment. Opening of effective band gaps can be achieved by field-effect in bilayer graphene, or by using Klein-tunneling properties of graphene p-n junctions. However, these methods appear not to effectively scale to small dimensions. Another way to open band gaps in graphene is to make graphene nano ribbons (GNRs) and use size quantization. Though many of the properties of 2D graphene are lost in the process, GNRs become similar to semiconducting carbon nanotubes, but with planar structures and compatibility with conventional lithographic processes. In this talk, I will present our group's research progress in making such wafer-scale GNR transistors. Band gaps ~0.15 eV appear in ~10 nm wide single GNRs, and band gaps are preserved in parallel arrays of GNRs. Based on these GNRs, we measure current drives as high as 10mA/micron, which far exceeds all other semiconductor materials and seems attractive for both logic and interconnect applications. The effects of edge roughness on scattering and mobility, and the progress towards making GNR-based tunneling transistors will also be presented.

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