Electronic Materials and Processing
Room: 9 - Session EM-TuM

Electrical Testing and Defects in III-V's
Moderator: E.M. Vogel, Georgia Institute of Technology, E.X. Zhang, Vanderbilt University

8:00am **EM-TuM1 Characterization, Modeling and Control of Fermi Level Pinning Phenomena at III-V High-k MOS Gate Stack Interfaces**, ***H. Hasegawa***, Hokkaido University and RIKEN, Japan **INVITED**

III-V high mobility channel materials are currently drawing attention as possible material candidates for devices to continue scaling of CMOS transistors on the Si platform. Here, construction of high performance high-k MOS gate stacks is the key issue. Such gate stacks are also needed for various gate controlled III-V nanowire and nanodot devices for "Beyond CMOS" applications.

The purpose of this paper is to review the present status of understanding and control of "Fermi level pinning (FLP)" phenomena at III-V metal-gate high-k gate stack interfaces whose atomic level control is vitally important for success of above approaches. FLP at the insulator-semiconductor (I-S) interface deteriorates efficiency and stability of gate control of carriers while FLP at the metal-insulator (M-S) interface deteriorates the control capability of the threshold voltage of the MOSFET.

First, various models on FLP at I-S and M-S interfaces are reviewed, paying attention to chemical trends of pinning at Schottky barriers and MOS capacitors formed on GaAs and other III-V materials. Extremely complicated C-V behavior of ALD high-k dielectric/GaAs MOS capacitors is explained by the authors' disorder induced gap state (DIGS) model [1] where a U-shaped donar-acceptor gap state continuum causes pinning. Importance of the location of the charge neutrality level (CNL) [2] is pointed out for channel material selection, showing superiority of InGaAs over GaAs and others.

Then, various efforts to remove FLP at III-V I-S interfaces by inserting interface passivation layers are reviewed. In particular, authors' efforts to realize pinning-free high-k MOS interfaces on GaAs and InGaAs, using the silicon interface control layer (Si ICL) are described. Here, the Si ICL is an MBE-grown ultrathin Si interlayer which is proposed first by the authors [2,3] and now extended to construction of high-k MOS gate stacks. The structure has been investigated by XPS, contactless C-V and STM/STS methods and by ex-situ PL and MOS C-V measurements [4-7].

Finally, the FLP issue at metal-high-k Schottky interfaces is briefly discussed.

[1]H. Hasegawa and H. Ohno, J. Vac. Sci.Technol, B**4**, 1130 (1986) [2]H. Hasegawa, M. Akazawa et al J. Vac. Sci. Technol. **B 7**, 870 (1989).[3]H. Hasegawa, M. Akazawa, et alJpn. J. Appl. Phys.. **27**, L2265 (1988) [4]M. Akazawa and H. Hasegawa, J. Vac. Sci. Technol. **B25**, 1481(2007)[5]M. Akazawa and H. Hasegawa, J. Vac. Sci. Technol. **B26**,(2008)1569 [6]M. Akazawa, A.Domanowska, B. Adamowicz and H. Hasegawa, J. Vac. Sci. Technol. **B27,** 2028(2009) [7]M. Akazawa and H. Hasegawa, Appl. Surf. Sci., **256,** 5708(2010)

8:40am **EM-TuM3 An Investigation into the Origin of Anomalous Frequency Dispersion in Accumulation Capacitance of MOS Devices on III-V Substrates**, ***R.V. Galatage***, *D.M. Zhernokletov, H. Dong, B. Brennan, C.L. Hinkle, R.M. Wallace,* University of Texas at Dallas, *E.M. Vogel*, Georgia Institute of Technology

Anomalous frequency dispersion in accumulation is a commonly observed feature in experimental capacitance-voltage (C-V) characteristics of III-V metal-oxide-semiconductor (MOS) devices. Different models have been proposed to explain the origin of this frequency dispersion. One model attributes this dispersion to tunneling of the carriers into a disordered region caused by oxidation of the III-V substrate which is close to the interface between the III-V substrate and an insulator.[1,2] Another model attributes this dispersion to border traps located inside the high-k dielectric.[3,4] In this work, we use both HfO_2 and Al_2O_3 with several interface treatments to differentiate between these two models.

MOS capacitors are fabricated on As-decapped n-$In_{0.53}G_{0.47}As$ and n-GaAs substrates with either atomic layer deposited (ALD) HfO_2 or Al_2O_3 dielectrics. An As-cap initially grown on the n-$In_{0.53}G_{0.47}As$ surface to avoid spurious oxidation is thermally desorbed to leave a pristine surface. ALD HfO_2 and Al_2O_3 is then deposited onto substrates prepared with several conditions: (1) *in situ* on the oxide free surface, (2) *ex situ* with a 10% ammonium sulfide and immediate transfer to ALD (<3 min exposure to air), (3) *ex situ* with a 10% ammonium sulfide treatment and ~30 min exposure to air prior to ALD. Companion GaAs samples receive similar *ex situ* ammonium sulfide treatments, air exposure times and ALD dielectrics for comparison. A detailed analysis of the effect of the different disordered region thicknesses and different dielectrics on the accumulation frequency dispersion and interface trap density (D_{it}) distribution will be presented. Correlation of electrical results to X-ray photoelectron spectroscopy (XPS) analysis will also be presented.

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[2] A. M. Sonnet, C. L. Hinkle, H. Dawei, G. Bersuker, and E. M. Vogel, IEEE Trans. Electron Devices, 57, 2599 (2010).

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[4] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett.96 (1), 012906 (2010).

9:00am **EM-TuM4 Evaluation of Atomic Layer Deposited High-k Dielectrics on GaAs**, ***H.J. Lim***, *Y.J. Choi, S.H. Lee,* Seoul National University, Republic of Korea, *J.H. Ku, N.I. Lee,* Samsung Electronics Co. Ltd., Republic of Korea, *H.J. Kim*, Seoul National University, Republic of Korea

GaAs is a promising channel material for sub-20nm logic MOSFET due to high electron mobility. However the instability of its native oxide is considered to generate high density of interface states that can induce Fermi level pinning and frequency dispersion in capacitance-voltage (C-V) curve. Although a variety of dielectric materials have been investigated over the past 4 decades to improve interface properties, a few positive results have been reported: $Ga_2O_3(Gd_2O_3)$ grown by molecular beam epitaxy (MBE) and Al_2O_3 and HfO_2 grown by atomic layer deposition (ALD). In this study, n-type GaAs MOSCAP's were fabricated with ALD SiO_2, Al_2O_3, La_2O_3, and HfO_2, and measurements of C-V hysteresis, flatband voltage shift (ΔV_{fb}), and frequency dispersion were performed to investigate the dependence of electrical properties on dielectric materials and to find dielectrics suitable for a stable MOSCAP operation.

Only HfO_2 revealed good electrical characteristics with a C-V hysteresis of < 80 mV and ΔV_{fb} of 40 mV under constant stress time and voltage, while SiO_2, Al_2O_3, and La_2O_3 showed significantly degraded characteristics with a C-V hysteresis of > 700mV hysteresis and ΔV_{fb} of 200mV. But even though a single HfO_2 dielectric layer had good electrical characteristics, the stacked HfO_2/SiO_2 dielectric layer on GaAs showed the degraded characteristics like a single SiO_2 layer, indicating that the electrical characteristics were mainly dependent not on bulk properties but on the interface properties with GaAs. X-ray photoelectron spectroscopy (XPS) analysis revealed that SiO_2, Al_2O_3, and La_2O_3 dielectrics produced more elemental As (As^0) than HfO_2 did at the interface. In addition, for SiO_2, Al_2O_3 and La_2O_3 dielectrics, As were detected on the top surface of dielectrics by Auger electron spectroscopy (AES) measurement, implicating that the origin of degradation was related with the amount of elemental As, which might diffuse out and induce vacancy defects during subsequent annealing process, at the interface.

Frequency dispersion characteristics in a C-V measurement were also compared. HfO_2 showed huge frequency dispersion of about 280 % ($\Delta C_{1kHz\sim1MHz}/C_{1MHz}$) while SiO_2, Al_2O_3, and La_2O_3 resulted in the relatively small dispersion of about 50% unlike the C-V hysteresis tendency. However, HfO_2 on thin SiO_2 led to small dispersion similar to SiO_2. Frequency dispersion was strongly correlated with the interface state density (D_{it}). Therefore, we can conclude that both hysteresis and frequency dispersion in a C-V measurement are dependent on the interface properties of dielectrics, especially the amount of elemental As and Dit level, respectively.

9:20am **EM-TuM5 High Energy XPS and Electrical Characterisation Studies of Metal Oxide Semiconductor Structures on Si, GaAs and InGaAs**, ***G.J. Hughes***, *L.A. Walsh,* Dublin City University, Ireland, *P.K. Hurley, J.H. Lin,* Tyndall National Laboratory, Ireland, *J.C. Woicik*, National Institute of Standards and Technology **INVITED**

In this work synchrotron radiation based hard x-ray photoelectron spectroscopy (HAXPES) measurements have been used to study the intrinsic electronic properties of high-k dielectric metal oxide semiconductor (MOS) structures on Si, GaAs and InGaAs substrates. The

MOS structures were prepared with both high (Ni) and low (Al) workfunction metal layers 5nm thick on both n and p doped semiconductor substrates. CV and IV measurements were also performed on an identical sample set where the top metal contact was 160 nm thick to facilitate electrical measurements, and Ni was replaced with Ni/Au, 70/90 nm thick, respectively. The 4150 eV photon energy used in the HAXPES measurements gave a photoemission sampling depth of ~15 nm ensuring that signals were simultaneously detected from the substrate, the 8 nm thick dielectric layers as well as the top metal contact. The binding energy of core levels in photoemission are referenced with respect to the Fermi level, therefore changes in the binding energy of a particular core level reflect differences in the position of the Fermi level in the semiconductor band gap. For the MOS structures fabricated using SiO_2/Si, changes in the Fermi level positions and differences in the potential drops across the dielectric layers have been directly correlated with the metal workfunction differences observed in the CV and GV measurements. The MOS structures on ammonium sulphide passivated n (Si - $5x10^{17}$ cm^{-3}) and p (Zn - $5x10^{17}$ cm^{-3}) doped GaAs substrates were fabricated by the atomic layer deposition (ALD) of 8 nm thick Al_2O_3 dielectric layers. A binding energy difference of 0.6 eV was measured between the GaAs core levels of the n and p doped substrates, independent of metal work function indicating that the Al_2O_3/GaAs interface is strongly pinned. Lattice matched 0.2 µm thick $In_{0.53}Ga_{0.47}As$ layers, with both n and p doping (~$4x10^{17}$ cm^{-3}), were grown by MOCVD on InP n^+ and p^+ substrates, respectively. Al_2O_3 dielectric layers 8 nm thick were then deposited ex-situ by ALD on the native oxide and ammonium sulphide treated InGaAs surfaces. Binding energy measurements for the core levels of native oxide covered n-type doped InGaAs substrates with no metal cap were found to be consistently (~0.3 eV) higher than p-type samples reflecting the fact that the Fermi level is in a different position in the band gap. Deposition of the metals with different workfunctions resulted in limited movement of the Fermi level, indicating the partially pinned nature of the InGaAs/Al_2O_3 interface. Corresponding changes in the potential across the dielectric layer were also measured.

10:40am **EM-TuM9 Metastable Centers and Localized States in AlGaN/AlN/GaN Heterostructures Studied by C-V, Admittance Spectroscopy, and DLTS**, ***A.Y. Polyakov***, *N.B. Smirnov*, *A.V. Govorkov*, *E.A. Kozhukhova*, Institute of Rare Metals, Russian Federation, *S.J. Pearton*, *F. Ren*, *L. Lu*, University of Florida, *S.Y. Karpov*, Soft-Impact, Ltd, Russian Federation, *W. Lim*, Samsung LED, Republic of Korea

A set of AlGaN/AlN/GaN high electron mobility transistor (HEMT) structures with Al composition in the AlGaN barrier changing from 20% Al to 50% Al was grown by metalorganic chemical vapor deposition (MOCVD) on sapphire and studied by means of capacitance-voltage C-V measurements, admittance spectroscopy, reverse deep levels transient spectroscopy. C-V and admittance measurements were performed in the dark and after illumination. The results suggest the presence in the AlGaN barriers of deep negatively charged traps of high concentration measurably shifting C-V characteristics to more positive voltages. The density of negatively charged centers can be increased by cooling at high reverse bias. These centers are believed to have a relatively high barrier for capture of electrons. Their thermal activation energy is estimated as 0.6-0.85 eV, the optical ionization energy is close to 1.7 eV. The presence of such centers explains lower than expected from modeling threshold voltages of the studied structures. Admittance spectroscopy also reveals consistent presence of features corresponding to apparent activation energy 0.11-0.13 eV for measurements at reverse voltages corresponding to a peak in AC conductance dependence on bias. These peaks in conductance and steps in admittance were attributed to transitions from the ground state in the triangular well near the AlN/GaN interface to the quasi continuum of excited states in the well with subsequent thermal emission into the conduction band. For samples illuminated at low temperature admittance spectra show unusual peaks in conductance with the activation energy close to the activation energy of thermal emission from the traps responsible for persistent photoconductivity.

11:00am **EM-TuM10 Characterizations of Proton-irradiated GaN and 4H-SiC by KOH Etching**, ***H.-Y. Kim***, Korea University, *Y.J. Shin*, *W. Bahng*, Korea Electrotechnology Research Institute, *J. Kim*, Korea University

We investigated the variations of the free electron concentrations and the etch pits such as threading screw dislocation (TSD), threading edge dislocation (TED) and mixed dislocation on proton-irradiated GaN and 4H-SiC. High energy protons create the radiation-induced defects (RD) such as single V_{Si}, V_C and interstitials, which can act as the carrier traps. Before proton irradiation, the energy loss and the penetration depth of the high-energy protons were assessed by Monte Carlo simulation (SRIM). Proton irradiations were performed on the sidewall and backside (carbon face of 4H-SiC) of the samples to examine the experimental proton-penetration depth. The irradiated fluence of the 6 and 8 MeV protons were $5x10^{15}$ cm^{-2}. High-energy protons gradually loss their energy by Coulomb interactions until they approach to specific depth where protons collide with the lattice atoms and create the point defects. The free electron concentrations of pre-irradiated GaN and 4H-SiC were $4x10^{16}$ cm^{-3} and $5x10^{18}$ cm^{-3}, respectively. The free carrier concentrations of proton irradiated GaN and SiC showed less than $1x10^{16}$ cm^{-3}, which can be calculated from the Raman scattering. After proton irradiation, 4H-SiC was etched in molten KOH at 530 ℃ for 3 min to compare the shape of the etch pits before and after proton irradiation. It was reported that the different kinds of etch pit were apparently distinguished at low-doped SiC, while the classification of the etch pit on highly doped SiC were very difficult. We observed the effect of the free carrier concentrations to the shape and the size of the etch pits. The results of molten KOH etched proton irradiated 4H-SiC showed different etch pits which were clearly distinguished. The TSDs were approximately 2-3 times larger than TEDs in proton-irradiated sample. After 1700 ℃ thermal annealing, the free electron concentrations were partially recovered. The differences of TEDs and TSDs were less evident after thermal annealing due to the recovery of the free electron concentrations. More details will be discussed.

11:20am **EM-TuM11 Trapping Centers in High -k Dielectrics for MOS Devices**, ***P. Lenahan***, Pennsylvania State University **INVITED**

This presentation will review experimental evidence with regard to trapping centers in high dielectric constant gate stacks in metal oxide semiconductor (MOS) devices. The presentation will deal primarily with hafnium oxide based systems on silicon. The presentation will include discussion of silicon/dielectric interface traps, trapping centers within the interlayer dielectric between the silicon and the high -k material, and defects in hafnium oxide. Most of the experimental evidence with regard to the physical and chemical nature of these trapping centers comes from electron paramagnetic resonance (EPR) and electrically detected magnetic resonance (EDMR). The presentation will thus emphasize EPR and EDMR measurements along with "electronic" measurements on these systems. An attempt will be made to link device processing, defect structures, and defect densities to the electronic proprieties of these high -k MOS systems.

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