Electronic Materials and Processing
Room: 9 - Session EM-TuA

Materials and Processes for Advanced Interconnects

Moderator: J. Bielefeld, Intel Corporation, S. King, Intel Corporation

2:00pm **EM-TuA1 Interface Engineering of Porous and Non-Porous ILD Layers Using Molecular Layer Deposition for Interconnect Applications**, ***J. Bielefeld***, Intel Corporation, *H. Zhou*, *P. Loscutoff*, Stanford University, *S. Clendenning*, Intel Corporation, *S.F. Bent*, Stanford University

As the dimensions continue to scale in interconnect processing, having a stable and controlled interface between the metal line and the dielectric material becomes more and more important. Molecular Layer Deposition (MLD) has been investigated as a method of growing thin films on dielectric surfaces which act as metal barriers, as blocking layers and as adhesion promoters. The advantage of MLD growth over conventional self-assembled monolayer (SAM) processing is the ability of MLD to easily grow films of varying thickness with tunable chemical functionality.

In this paper, we will discuss the growth and thermal stability of poly-urea-based MLD thin films on both porous and non-porous Carbon Doped Oxide (CDO) dielectric surfaces and compare this work to similar MLD films grown on conventional SiO_2. A variety of characterization techniques, including thermal stress test, secondary ion mass spectrometry, x-ray photoelectron spectroscopy, and electron microscopy, were used to determine film composition, film stability, film adhesion, and degree of penetration into porous substrates. We investigate the importance of surface preparation on the anchoring of MLD films to CDO surfaces. Surface preparation is especially important when growing controlled layers on the surface of a porous dielectric, and we show that surface treatments influence the depth of penetration of the MLD film within porous CDO. Finally, we examine the deposition of thin metal films on top of MLD coated CDO layers (both blanket and patterned) and we show that the metal deposition process impacts both the MLD stability and the metal penetration into the ILD.

2:20pm **EM-TuA2 Synchrotron X-ray Scattering Investigation of Morphological Stability of Cu Thin Film Interfaces**, ***A.P. Warren***, University of Central Florida, *M.F. Toney*, Stanford Synchrotron Radiation Lightsource, *K. Barmak*, Carnegie Mellon University, *I.I. Kravchenko*, Oak Ridge National Laboratory, *K.R. Coffey*, University of Central Florida

Nanometric films of pure Cu continue to attract attention due to their widespread use as interconnect material in the semiconductor community. Among the various engineering and scientific challenges posed by the continued use of Cu is its high surface mobility, which is well known to result in both elecromigration and stress induced void formation in interconnects. The use of barrier/adhesion layers greatly improves the reliability of Cu interconnects. Nonetheless, the diffusion of Cu along the Cu/barrier interface is not well understood. Addressing the thermal stability and morphological evolution of Cu/barrier interfaces with the intent of quantifying interfacial diffusivities is the ultimate goal of this research.

Synchrotron x-ray scattering was used to study the evolution of interface roughness with annealing for a series of Cu thin films. The films were encapsulated in SiO_2 or Ta / SiO_2 and prepared by sputter deposition. Specular x-ray reflectivity was used to determine the root mean square roughness for both the upper and the lower Cu / SiO_2 (or Cu / Ta) interfaces. The lateral roughness was studied by diffuse x-ray reflectivity. Annealing the films at 600°C resulted in a smoothing of only the upper interface for the Cu / SiO_2 samples, while the lower Cu / SiO_2 interfaces and both interfaces for the Ta encapsulated films did not evolve significantly. As a function of roughness wavelength, the upper Cu / SiO_2 interfaces exhibited a roughness decay with annealing that was only 12.5% of that expected for classical capillarity driven smoothening of a free surface.

Continued work is focusing on further quantifying the interface kinetics for Cu/barrier systems. Using e-beam lithography methods, we have patterned a grating onto the surface of Cu thin films. Subsequent encapsulation and annealing will be carried out to study the effects of time and temperature on the patterned interface.

2:40pm **EM-TuA3 Interconnect Scaling for 10nm and Beyond**, ***Z. Tokei***, IMEC, Belgium **INVITED**

The rapid introduction of different interconnect schemes enabled sustained scaling towards advanced technology nodes. Enablers are dimensional and material scaling together with system level aspects. Both logic and memory chips require tight pitch interconnecting lines with some common aspects and at the same time some different requirements. From material and dimensional scaling point of view logic interconnects demand tight pitch metal lines with low-k dielectrics, while emerging memories demand high current (or voltage) through tight pitch metal lines embedded into silicon oxide or air gaps. Conventional interconnects are built using multilevel damascene recently added with multiple patterning techniques leading to increased complexity. In order to break down the barrier and pave the way for 10nm technologies and beyond further material innovation along with non-conventional integration schemes and potentially system architecture modification will be necessary. Copper interconnects will require less than 2nm cladding layer or eventually the complete omission of conventional Ta-based diffusion barriers. Copper based metallization is expected to extend to 15nm critical dimensions although the number of elements through alloying and various liners increases already today. At 10nm and below alternatives to Cu wiring without a reliability issue is a candidate. For thin film deposition self assembled mono-layers, electroless and CVD/ALD techniques are becoming important, while novel dielectrics increasingly rely on self-assembling chemistries. This talk will focus on options that are being considered for 10nm and beyond. While several aspects will be mentioned, the main emphasis will be put on material innovation. Examples and case studies will be detailed for dielectric and metal options along with the relevant material characterization. Examples include defect characterization in low-k materials, phase identification and stress measurements in metal lines.

4:00pm **EM-TuA7 High Throughput Crystal Orientation Mapping of Nanometric Cu: Impact of Surface and Grain Boundary Scattering on Electrical Resistivity**, *X. Liu*, Carnegie Mellon Univ., *A. Darbal*, Nanomegas, *K. Ganesh*, Univ. of Texas at Austin, *G. Rohrer*, *D. Choi*, Carnegie Mellon Univ., *P. Ferreira*, Univ. of Texas at Austin, *B. Yao*, *T. Sun*, *A.P. Warren*, Univ. of Central Florida, *M.F. Toney*, Stanford Synchrotron Radiation Lab, ***K.R. Coffey***, Univ. of Central Florida, *K. Barmak*, Carnegie Mellon Univ.

Due to limitations in characterizing twin boundaries in nanocrystalline Cu, it has been difficult to account for twin boundary scattering in the quantitative analysis of the resistivity size effect. In this study, a recently developed high throughput electron diffraction based metrology method in the transmission electron microscope, known as ASTAR™, is employed to obtain crystal orientation maps in two SiO_2 and 6 $SiO_2/Ta_{38}Si_{14}N_{48}$ encapsulated nanocrystalline Cu thin films. In ASTAR™, a dedicated hardware unit is used for precession and automated scanning of a nanosized quasi-parallel electron beam probe. A high speed external optical camera is then used for rapid acquisition of spot diffraction patterns. The acquired spot patterns are indexed automatically using a template matching algorithm. Significant improvement in the reliability of the orientation maps is achieved with electron beam precession. The use of precession reduces the dynamical effects and increases the number of spots in the diffraction pattern. The use of rapidly acquired spot patterns and the robust template matching algorithm make ASTAR™ highly suitable for obtaining large datasets of crystal orientations. Analysis of the orientation maps of the Cu films shows a significant fraction of incoherent twin boundaries, indicating a potentially higher resistivity contribution from twin boundary scattering than previously assumed. Including the mixture of coherent and incoherent twin boundaries in the study of the resistivity size effect shows that the contribution from grain boundary scattering is still the dominant resistivity size effect in Cu, compared to surface scattering. Inclusion of the twin boundary mixture in a quantitative model shows the resistivity data to be best described by the Fuchs Sondheimer surface scattering model and the Mayadas Shatzkes grain boundary scattering model, combined using Matthiessen's rule (simple summation), with a surface specularity coefficient, $p = 0.50$, and a grain boundary reflection coefficient, $R = 0.26$. These values can be compared with values of $p = 0.52$ and $R = 0.43$ obtained in previous studies where the presence of twin boundaries was not considered. The potential to separately quantify electron scattering at twin boundaries and non-twin grain boundaries, the role of surface roughness, measured by x-ray reflectivity using synchrotron radiation, and the role of voids, measured using high angle annular dark field imaging in the transmission electron microscope, will also be discussed.

4:20pm **EM-TuA8 Developing Robust Ultra-Low-k Dielectric (κ≤2.55) Materials using Novel Characterization Techniques for the 20nm Node and Beyond**, *D.R. Kioussis*, ***Z. Sun***, *Y. Lin*, GLOBALFOUNDRIES, *A. Madan*, *N. Klymko*, *C. Parks*, *S. Molis*, IBM Semiconductor R&D Ctr, *E.T. Ryan*, GLOBALFOUNDRIES, *E. Huang*, *S.M. Gates*, *A. Grill*, IBM T.J. Watson Res. Center, *B. Kim*, *J.K. Kim*, Samsung Electronics Co. Ltd., Korea, *D. Restaino*, *T.H. Lee*, IBM Semiconductor R&D Ctr, *S. Hosadurga*, IBM Research Group, *S.A. Cohen*, IBM T.J. Watson Res. Center, *K. Virwani*, IBM Research - Almaden

As the semiconductor industry pushes feature miniaturization limits beyond the 20nm node, novel interline dielectric materials with low dielectric constants (k-value), so called ultra low-k (ULK) materials (k < 2.55), are targeted to prevent capacitive crosstalk, interline leakage and reduced power consumption of advanced integrated circuits (IC). These materials are commonly porous (>15%) and organic in nature, which necessarily incur compromises in either the thermal or mechanical integrity with respect to more traditional dense low-k and SiO2 dielectrics. Porous organosilicate glass ULK films with k-values 2.4 - 2.55 deposited by PECVD and cured via UV irradition were first put into production at the 45nm node to further minimize RC delay. These ULK materials incorporate a large number of methyl (Si-CH_3) groups and pores into Si-O based network structures. The methyl groups disrupt the Si–O bond network, which tend to lower density and also lower polarizability making the film hydrophobic. Lower density, reduced polarizability, and greater hydrophobicity decrease the k-value. Introduction of porosity is used to further lower the k-value but other critical film properties, such as fracture toughness are affected. A viable ULK material must survive "damage" sustained from a series of processing steps that include dual-damascene (DD) litho, RIE, stripping and cleaning, CMP, and packaging. The reliability of devices containing these multi-layer DD stacks depends heavily on the chemical and mechanical stability of the dielectric, as this is the material and structural template in which the IC functionality is laid. Damage mechanisms occur when ULK is exposed to RF-plasma during etching or ashing. Subsequent moisture adsorption leads to the increase of effective k-value degrading performance. The integration challenges of ULK are significant, such as plasma damage, chip packaging, and ILD/metal barrier compatibility issues. Substantial optimization of the ULK properties via quick turn methods is crucial for successful integration in advanced 20 nm generations. This study will discuss optimization of the material properties of single or dual precursor based ULK films through the use of different process chemistry and tuning of material deposition and UV curing parameters to meet the integration and packaging requirements. Quick turn characterization techniques were used to determine critical film properties. Correlation between film properties to the degree of plasma damage and mechanical integrity of ULK will be shown. We will show that careful modification of the ULK properties to minimize damage resulted in the successful integration at the 20nm node.

4:40pm **EM-TuA9 Reflection Electron Energy Loss Spectroscopy Investigation of Band Gap and Defect States in Low-k and High-k Dielectrics**, ***B. French***, *S. King*, Intel Corporation

Electrical leakage in high-k metal gate transistors and low-k/Cu interconnect structures is a growing, vital concern as the nano-electronics industry moves to sub-16 nm technology nodes and continues to implement new materials. In order to understand the various possible leakage mechanisms in low-k/Cu interconnects, knowledge of the band gap and defects states in low-k and high-k dielectrics is needed but has gone largely unreported in many cases. In this regard, we have utilized Reflection Electron Energy Loss Spectroscopy (REELS) to determine the band gap of numerous single crystalline and amorphous low-k and high-k dielectric materials. We demonstrate that for standard single crystalline materials such as Quartz, 6H-SiC, and GaN, REELS band gap measurements agree with known values. For amorphous low-k and high-k thin film materials, we further demonstrate that REELS band gap measurements in most cases agree with optical measurements of the same materials. However in some cases, we have observed that the REELS analysis can be complicated by the existence of defect states within the band gap of these materials. While troublesome for band gap measurements, we demonstrate that this sensitivity can be utilized to determine the energy level of various defects in pristine and sputter damaged low-k SiOC:H dielectrics and in some cases identify the chemical identity of the defect.

5:00pm **EM-TuA10 The Effects of Plasma Exposure and Vacuum-Ultraviolet Radiation on Photopatternable Low-k Dielectric Materials**, ***M.T. Nichols***, *K. Mavrakakis*, University of Wisconsin-Madison, *Q. Lin*, IBM T.J. Watson Research Center, *J.L. Shohet*, University of Wisconsin-Madison

Silsesquioxane-based photopatternable low-k (PPLK) dielectric materials[1] are promising alternatives to existing low-k dielectrics due to the reduction of BEOL integration complexity. However, processing-induced damage due to reactive species and energetic particles has been previously found to be problematic for low-k organosilicate dielectrics. Thus, for successful integration, the effects of charged-particle bombardment and photon irradiation (particularly in the vacuum ultraviolet range) must be characterized. In order to examine these effects, I-V and C-V characteristics were made on PPLK samples before and after exposure to a variety of argon plasma exposure conditions. Plasma parameters were varied between each exposure so that each sample was subjected to a range of charged particle and photon fluxes. In order to examine the effects of photon irradiation alone, PPLK samples were also exposed to monochromatic synchrotron radiation over energies varying from 5 to 15 eV. It was found that both charged-particle bombardment and photon irradiation have deleterious effects, resulting in increased magnitude of leakage currents and increased flat-band voltage shifts. VUV-exposed samples also exhibited increased leakage currents, but this effect was found to be strongly dependent on photon energy.

This work has been supported by the Semiconductor Research Corporation under Contract 2008-KJ-1871 and by the National Science Foundation under Grant CBET-1066231.

[1] Q. Lin, S.T. Chen, A. Nelson, et al., **Proc. Of SPIE** 7639, 76390J (2010)

5:20pm **EM-TuA11 A Survey of Alternative Methods for Curing Porous SiCOH Films**, ***N. LiCausi***, *V. Kamineni*, GLOBALFOUNDRIES, *S. Ohsiek*, *H. Geisler*, *M. Weisheit*, *M. Majer*, GLOBALFOUNDRIES, Germany, *E.T. Ryan*, GLOBALFOUNDRIES

SiCOH films have been used in advanced semiconductor devices to enable continued scaling of interconnect integration. The further scaling of ultra low *k*-value (ULK) films has necessitated a move to porous SiCOH films. Porosity is intentionally introduced to decrease the dielectric *k*-value and therefore reduce interconnect RC delay. However, this porosity also leads to reduced mechanical strength and presents substantial challenges to integration and packaging.

Nanoporous thin films can be formed with PECVD of a SiCOH film with embedded porogen clusters. The porogen can either be supplied by a second porogen precursor or using a single precursor containing an embedded porogen fragment. The porogen is then removed with curing. Currently the industry favors UV assisted thermal curing to simultaneously drive out porogen (forming the porous structure) and enable cross-linking of the film matrix (Si-O-Si bond formation). However, prior investigation claims that this porogen is not completely removed, leaving porogen residue in the pores [1]. It is believe that cross-linking of the film matrix inhibits porogen removal and inversely, porogen residue prevents efficient cross-linking. Subsequently, this can lead to degraded electrical and mechanical performance.

A new approach under review uses a two-step curing procedure. First porogen is removed from the film with a novel film treatment. This step targets porogen removal, but does not cross-link the film's matrix. An example of this is remote H_2/He plasma (H radical exposure) [2]. After removing the porogen, a traditional UV assisted thermal cure strengthens the film and drives out any remaining porogen. We evaluated this and two similar approaches and observed the same qualitative trends. Generally speaking, when using conventional curing techniques there is an unavoidable tradeoff between *k*-value and mechanical performance. However, the two-step process results in films which have both increased mechanical strength and improved electrical performance.

Films have been evaluated electrically (*k*-value, breakdown voltage, leakage current). Film structure (porosity and pore size distribution), mechanical properties (Young's modulus) and film composition were measured with ellipsometry porosimetry, nanoindentation and XPS/FTIR, respectively. The UV absorption peaks related to porogen residue have also been measured using vacuum ultraviolet spectroscopic ellipsometry.

[1] A.M. Urbanowicz, K. Vanstreels, D. Shamiryan, S.D. Gendt and M.R. Baklanova, *Electrochem. Solid St.***12** (2009).

[2] A.M. Urbanowicz, K. Vanstreels, P. Verdonck, D. Shamiryan, S. De Gendt and M.R. Baklanov, *J. Appl. Phys.***107** (2010).

5:40pm **EM-TuA12 Metallization Challenges in Integration of Soft Dielectric Materials**, ***R. Chebiam***, *C. Jezewski*, *B. Krist*, *H. Yoo*, *J. Clarke*, Intel Corporation

In order to take advantage of reduction in transistor gate delay at smaller dimensions, back-end interconnect (RC) delay has to be minimized. One of the methods of reducing the system capacitance is by reducing the dielectric constant of ILD's at each technology node. There is an observed trend that modulus and hardness of dielectric films degrades with decreasing k value. This is either due to increased carbon content or increased porosity. Ultra low-k materials (k<2.2) are well known to be susceptible to damage during the patterning process. However, there has been little focus on the damage resulting from the metallization process (barrier/seed, plate, and CMP).In

this study we use a spin-on dielectric (K~2.2) with E =4.5GPa and H= 0.3GPa to investigate metallization damage. The soft ILD shows little feature size blowout post metallization for large feature sizes (>100nm). However, features size blowout of ~10-18 % is seen for sub 100nm features post metallization compared to pre-metallization. Feature blow out appears to be driven by dielectric densification and to a less extent from material etch out. Densification damages the dielectric by increasing the k value and hence must be minimized. The origin of the feature size blowout can be traced to an energetic barrier or seed deposition process. For example, a high resputter PVD barrier process has similar blowout compared to an ALD Liner process. When the energy of barrier /seed process was decreased blowout was reduced, but this was accompanied by poorer sidewall coverage which will result in degraded gapfill and reliability. The key challenge can then be highlighted as developing a low energy barrier/seed process that has good sidewall coverage (conformality) and no feature blowout to enable ultra low-k dielectrics integration.

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