Electronic Materials and Processing
Room: 9 - Session EM+TF+OX+GR-MoM

High-k Dielectrics for MOSFETs I
Moderator: A.C. Kummel, University of California San Diego

8:20am **EM+TF+OX+GR-MoM1 Surface Preparation and Dielectric Growth for Graphene-based Devices**, ***R.M. Wallace***, University of Texas at Dallas **INVITED**

In addition to interesting physics, numerous device applications are under investigation for graphene. Many of these devices require an interaction of graphene with dielectrics, and require a thorough understanding of the graphene/dielectric interface. As practical device applications require large area graphene, CVD methods have been employed to synthesize graphene and typically involve a wet chemical transfer process, which can leave residues that impact device behavior. This talk will review recent progress in the investigation of CVD graphene growth, transfer and dielectric growth processes with an emphasis on in-situ studies of the surfaces produced by these processes and the resultant electrical behavior. This work is supported by the NRI SWAN Center.

9:00am **EM+TF+OX+GR-MoM3 Antimonide-Based P-Channel MOSFET: Progress and Challenges**, ***S. Oktyabrsky***, *A. Greene, S. Madisetti, P. Nagaiah, M. Yakimov, R. Moore, S. Novak, H. Bakhru, V. Tokranov*, University at Albany-SUNY **INVITED**

Development of p-type MOSFETs using new materials is an important goal to provide a further scaling of CMOS circuits. Although Ge is still considered as a main candidate for novel p-channels due to its superior bulk transport properties, recent progress in strained III-Sb channels and MOS technologies makes it a good competitor in particular for deeply scaled devices. The materials parameters affecting MOSFET's figures-of-merit are reviewed with the emphasis on strain in quantum wells (QWs), effective mass, density of states and mobility.

Progress in development of materials for III-Sb channels is reported. Optimization of MBE growth of metamorphic buffers and GaSb on lattice-mismatched GaAs substrates has resulted in "step-flow" growth mode of GaSb with monolayer-high steps on the surface, ~10^7cm^{-2} dislocation density and bulk hole mobility 860cm^2/Vs. Optimization of strain in QWs provided the highest Hall mobility of 1020 cm^2/Vs at sheet hole density of 1.3x10^{12}/cm^2 obtained for $In_{0.36}Ga_{0.64}Sb$ with compressive strain of 1.8%. Hole mobility in QW channel was benchmarked against the thickness of top semiconductor AlGaSb barrier. The effect of interface-related scattering hole mobility in the channel was found to be significantly less than e.g. for n-InGaAs, that might be due to stronger localization of holes in QWs.

Two approaches to fabricate high-quality III-Sb/high-k interface were studied: all *in-situ* Al_2O_3 or HfO_2 gate oxides, and *ex-situ* atomic layer deposited (ALD) Al_2O_3 with InAs top semiconductor capping layer. Interface with *in-situ* MBE gate oxides was found to improve with *in-situ* deposited a-Si interface passivation layer (IPL). Interfaces with better thermal stability, reduced interface trap density and hysteresis were observed on both n- and p- type GaSb MOSCaps with the IPL. P-type MOSFETs with HfO_2 showed a maximum drain current of 23 mA/mm for a 3μm gate length. Use of a-Si IPL has also resulted in a significant (over an order of magnitude) reduction of the hole density in QWs and corresponding negative flat band voltage shift and drop of mobility which becomes remote Coulomb scattering-limited. An interface with ALD Al_2O_3 was improved by a thin 2nm interface layer of InAs which was treated with HCl or$(NH_4)_2S$ immediately prior to ALD process. Optimized annealing further improved the C-V characteristics, reduced interface trap density down to 10^{12} cm^{-2}eV^{-1}, leakage current and MOSFET subthreshold slope down to 200 mV/dec. Increasing annealing temperature to and above 450^{o}C drastically degraded C-V characteristics due to low thermal budget of antimonides.

9:40am **EM+TF+OX+GR-MoM5 Interface Study of the Atomic Layer Deposited Al_2O_3 on $Al_{0.25}Ga_{0.75}N$**, ***X. Qin***, *B. Brennan, H. Dong, R.M. Wallace*, The University of Texas at Dallas

Due to the high two-dimensional electron gas (2-DEG) density, AlGaN/GaN high electron mobility transistors (HEMTS) are recognized as key devices for high power and low noise applications. However, the associated large gate leakage current degrades the performance of AlGaN HEMTs. In order to solve this problem, MOS-HEMTs have been developed, in which the incorporation of a high-k gate dielectric layer can overcome the drawbacks.

In this work, the native and treated $Al_{0.25}Ga_{0.75}N$ surface chemical states and structure of were studied by x-ray photoelectron spectroscopy (XPS), ion scattering spectroscopy (ISS) and low energy electron diffraction. Different chemical treatment processes including $(NH_4)OH$, $(NH_4)_2S$ and HF were studied, followed by atomic layer deposition (ALD) Al_2O_3 layers on $Al_{0.25}Ga_{0.75}N$. The oxidation states of the $Al_{0.25}Ga_{0.75}N$interface and Al_2O_3 deposition process were studied by in-situ XPS analysis. In addition, ex-situ atomic force microscopy (AFM) was used to observe the surface topography before and after the Al_2O_3 deposition. According to the XPS results, it is found that chemical treatments could remove the native Al_2O_3 but were not effective to eliminate the Ga oxide, and the growth rate of Al_2O_3 is low on the native and treated $Al_{0.25}Ga_{0.75}N$ samples. The AFM images show that there are many pin holes in the surface of $Al_{0.25}Ga_{0.75}N$. Studies of HfO_2 deposition will also be presented.

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10:00am **EM+TF+OX+GR-MoM6 Ideal Monolayer Nitridation of Semiconductors using a Nitrogen Radical Generator**, ***A.T. Lucero***, *J. Kim*, University of Texas at Dallas

Thin silicon nitride films have long been desirable for various applications. Suggested uses range from surface and interface passivation to ultra-thin dielectric layers. Traditional deposition techniques are low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD). High quality LPCVD films require high processing temperatures, and PECVD exposes the substrate to damaging plasma and electric potentials. While both techniques are suitable for many applications, there are some instances where both processes are too harsh.

In this paper, we report the growth of silicon nitride using a remote nitrogen radical generator system. Growth temperatures range from room temperature to 400 °C,and growth time is varied from two minutes to one hour. Film composition is analyzed using x-ray photoelectron spectroscopy (XPS) and morphology is checked using atomic force microscopy. Results indicate that surface nitrogen saturation can be reached at both low temperatures and short exposure times,and that the reaction is self limiting, terminating at one monolayer. Film thickness is approximately one Angstrom, as determined by XPS. Results for silicon and III-V passivation will be discussed.

We would like to thank Toshiba Mitsubishi-Electric Industrial Systems Corporation for providing the nitridation system used in this study.

11:00am **EM+TF+OX+GR-MoM9 Characterization of ALD Laminated Gate Dielectrics on GaN MOSCAPs**, ***D. Wei***, *T. Hossain*, Kansas State University, *N. Nepal, N.Y. Garces*, Naval Research Laboratory, *H.M. Meyer III*, Oak Ridge National Laboratory, *C.R. Eddy, Jr.*, Naval Research Laboratory, *J.H. Edgar*, Kansas State University

To improve the efficiency of GaN based power electronic devices there is tremendous and growing interest in employing metal-insulator-semiconductor (MIS) transistors. As with all compound semiconductors, there is a significant challenge in forming an electronic quality dielectric-semiconductor interface. Thus, there is a need to better understand and improve the dielectric-semiconductor interface quality in order to improve the overall performance of the device.

This research focuses on the benefits and properties of Al2O3, TiO2 and TiO2-Al2O3 nanolaminate thin films deposited on GaN and GaOx/GaN by plasma-assisted atomic layer deposition (PA-ALD) for gate dielectric development. Correlations were sought between the films' structure, composition, and electrical properties. The gate dielectrics were approximately 15nm thick as determined by spectroscopic ellipsometry. The interface carbon concentration, as measured by x-ray photoelectron spectroscopy (XPS) depth profile, was lower for Al2O3/GaN than TiO2/GaN, and the nanolaminate structure did not decrease the carbon concentration. However, carbon was not detected at the interface for the GaN samples pretreated by annealing in O2 for 30 minutes at 800°C. Also, according to XPS, the Al2O3 films had a better coverage than TiO2. The RMS roughness of TiO2 and Al2O3 top layers were ~0.53nm and ~0.20nm respectively, as determined by atomic force microscopy. The dielectric constant of Al2O3 on GaOx/GaN was greatly increased compared to that of the TiO2-Al2O3 and pure Al2O3 on GaN substrate. In addition, the Al2O3 deposited on the GaOx/GaN showing no hysteresis in capacitance-voltage (C-V) characteristics, which is corresponding with a negligible carbon concentration from the XPS depth profile. These results indicate the

promising potential of plasma ALD deposited Al2O3 serving as the gate oxide on GaOx/GaN based MOS devices.

11:20am **EM+TF+OX+GR-MoM10 Passivation of Interfacial Defects in GaAs and Other III-Vs**, ***J. Robertson***, Cambridge University, UK **INVITED**

It has always been harder to make FETs from GaAs than Si, because of 'Fermi level pinning' and the difficulty of passivating its surfaces. These issues were discussed by Spicer et al [1] in the 'unified defect model' and Hasegawa [2] is his 'Disorder Induced Gap states' model. Since 1997 it was possible to make inverted GaAs MOSFETs using the epitaxial Gadolinium gallium oxide [3]. The main impetuous now is to use atomic layer deposition (ALD) to make scalable FETs [4], as recently achieved by Intel [5]. The obvious question is why (In)GaAs is much harder to passivate than Si. The early answer was its poor native oxide. But since the advent of good ALD HfO2 or Al2O3 oxides on Si, this answer is deficient, as they should also work on GaAs [6]. The underlying reason for defects is not stress, it must be chemical. I show that it arises from the polar bonding of GaAs [7], and a driving force to keep the surface Fermi level in a gap. The electron counting rule of Pashley [8] that describes surface reconstructions is shown to be a variant of auto-compensation, and it works more generally [9]. It leads to a continuous generation of defects if it is not satisfied. So the answer is to deposit oxide layers that meet this rule, and also to break any surface reconstructions that may lead to As-As dimers [9]. Diffusion barriers are also crucial to a good passivant, on GaAs or on Ge .

1. W E Spicer, et al, J Vac Sci Technol 16 1422 (1979); Phys Rev Lett **44** 420 (1980)

2. H Hasegawa, et al, J Vac Sci Technol B 5 1097 (1987)

3. M Hong et al, Science **283** 1897 (1997)

4. P D Ye et al, App Phys Lett 83 180 (2003)

5. M Radosavljevic, et al, Tech Digest IEDM (2009) p13.1

6. C Hinkle, et al, Curr Opin Solid State Mat Sci 15 188 (2011)

7. W Harrison, J Vac Sci Technol 16 1492 (1979)

8. M D Pashley, Phys Rev B **40** 10481 (1989)

9. J Robertson, L Lin, App Phys Letts 99 222906 (2011); **98** 082903 (2011)

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