Electronic Materials and Processing
Room: 9 - Session EM+TF+OX+GR-MoA

High-k Dielectrics for MOSFETS II

Moderator: C.L. Hinkle, University of Texas at Dallas, H.J. Kim, National Institute of Aerospace (NIA)

2:00pm **EM+TF+OX+GR-MoA1 "6.1" Family: The Next Generation of III-V Semiconductors for Advanced CMOS: Epitaxial Growth and Passivation Challenges**, ***C. Merckling***, *A. Alian, A. Firrincelli, S. Jiang, M. Cantoro, J. Dekoster, M. Caymax, M. Heyns*, IMEC, Belgium **INVITED**

The integration of high carrier mobility materials into future CMOS generations is presently being studied in order to increase drive current capability and to decrease power consumption in future generation CMOS devices. If III-V materials are the candidates of choice for n-type channel devices, antimonide-based III-V semiconductors present the unique property of owning both high electrons (InSb) and holes (GaSb) mobilities, which triggered much of the interest in these III-Sb compounds for advanced CMOS. Moreover recent simulations have demonstrated that higher hole mobility could be found in strained III-antimonides compounds, suggesting the possibility of an all III-antimonide solution for full III-V based CMOS. In this work we studied the heteroepitaxy of 6.1 family semiconductors (GaSb, AlSb & InAs) on various III-V and Si substrates as well as the passivation of such semiconductors.

The relatively large lattice parameter of "6.1" semiconductors makes the growth and the integration on standard surfaces difficult. But is it possible to grow such semiconductors fully relaxed with low defect density due to the formation of a highly periodic array of 90º misfit dislocations at the III-Sb/substrate interface. In this contrbution both MBE and MOVPE growth techniques have been studied in order to propose novel integration scheme on Si substrate.

In a second part, we will focus on the passivation of these III-V semiconductors. Because III-V surfaces are very sensitive to oxygen compounds, this will generate the formation of native oxide. This undesirable interlayer will contribute aggressively to the high density of surface states within the energy band gap, resulting in Fermi level pinning which disturbs the basic III-V MOSFET-operation. In this context both ex-situ and in-situ Al_2O_3 high-κ gate dielectric deposition by standard ALD or MBD processes is reported. The interface is abrupt without any substantial interfacial layer, and is characterized by high conduction and valence band offsets. Finally, MOS capacitors showed well-behaved C-V with relatively low D_{it} along the band gap. Such a D_{it} profile is promising for the future devices and suggests possibility to attain a low subthreshold swing.

2:40pm **EM+TF+OX+GR-MoA3 Improving Nucleation and Passivation of Ge(100) via H_2O and H_2O_2 Dosing**, ***T. Kaufman-Osborn***, *K. Kiantaj, J.S. Lee, A.C. Kummel*, University of California San Diego

Germanium is a promising candidate for potential channel materials due to its higher hole and electron mobility. To minimize the oxide-semiconductor interfacial defect density, a proper passivation layer must be used before the oxide layer is deposited. In this study, a monolayer of H2O chemisorbates is shown to activate TMA chemisorption due to the Ge-OH bonds catalyzing the formation of an ultrathin passivation layer which can serve as an ideal ALD nucleation template on a Ge surface. However, since H2O chemisorption results in equal density of Ge-H and Ge-OH sites on the Ge(100), H2O can only provide a maximum of 0.5 monolayer of Ge–OH sites, limiting the TMA nucleation density. By using H2O2 dosing, the density of Ge–OH sites can be doubled thereby increasing the potential TMA nucleation density. This study compares the passivation of the Ge(100) surface via H2O and H2O2, for the application of nucleating ALD growth on the surface, using scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS).

A saturation H2O dose onto Ge(100) resulted in 0.85 ML coverage of –OH and –H species chemisorbed on the surface. The remaining unreacted atoms on the surface have half filled dangling bond states causing a large local amount of conduction band edge states in the bandgap. The Ge–OH and Ge–H sites on the surface have limited thermal stability. Annealing the H2O/Ge(100) sample to 100°C significantly reduces the H2O coverage due to the recombinative desorption of H2 or H2O.

A saturation dose of H2O2 on Ge(100) at 25oC results in a coverage of 0.95 ML of Ge–OH species chemisorbed on the surface with very few unreacted sites. Compared to a H2O dose, H2O2 provides more than double the number of reactive Ge-OH sites thereby increasing the number of potential ALD nucleation sites. In contrast to the H2O passivated surface, annealing the H2O2/Ge surface to 100°C generates no additional dangling bond sites and even eliminates the dangling bonds present from the 25oC dose and forms a highly ordered surface of Ge-OH bonds. The improved coverage of Ge–OH sites allows for increased nucleation density of O-Al bonds and also minimizes the dangling bonds which are considered as the major source of interfacial trap states (Dit). The improved thermal stability allows for an increased thermal budget during ALD cycles. STS measurements show that TMA nucleation on the H2O2 functionalized Ge(100) surface unpins the Fermi level and has a wide bandgap with no band edge states demonstrating very good interface quality.

3:00pm **EM+TF+OX+GR-MoA4 Electrical and Physical Characteristics of High-k/Metal Gate MOS Devices on MBE-Grown Germanium on Silicon Using Aspect Ratio Trapping**, ***S.R.M. Anwar***, *C. Buie, N. Lu, M.J. Kim, C.L. Hinkle*, University of Texas at Dallas

Due to its high hole mobility and relative compatibility with Si CMOS processing, Ge has long been considered as a replacement channel material for PMOS devices. Selective area growth of Ge channels on bulk Si substrates would be ideal for minimizing fabrication costs and allowing the co-implementation of other materials (III-Vs for NMOS). However, due to the 4.2% lattice mismatch between Ge and Si, unacceptably high dislocation densities (~10^9 cm^{-2}) are created during this heteroepitaxy.

In this work, we investigate the fabrication of MOS gate stacks on MBE-grown Ge on Si using Aspect Ratio Trapping (ART)[1,2] to reduce Ge defect density. ART is a growth technique that allows for the reduction of defects for lattice mismatched materials by trapping the threading dislocations into the sidewalls of patterned nanoscale trenches in which the epitaxial growth takes place. This technique has the added benefit of producing the necessary geometric structure required for highly scaled tri-gate devices while reducing defect density simultaneously. Surface roughness and defect density dependence on growth temperature and growth rate will be discussed as will be the effect of varying the trench geometry. RHEED, XRD, XPS, TEM, EPD, AFM, SEM, and IPE data are correlated with growth conditions to produce high quality heteroepitaxial growth. Data will be presented demonstrating the use of low-temperature buffer layers in conjunction with low-growth rate bulk Ge results in a reduction in threading dislocations of 2-3 orders of magnitude.

MOS devices were fabricated on the MBE-grown Ge on Si samples. A high-quality interface was obtained using a DI-H_2O surface functionalization by pre-pulsing the H_2O 50 times in the atomic layer deposition (ALD) chamber at 250 °C.[3] A thin interfacial Al_2O_3 film was deposited by ALD at 250 °C followed by forming gas anneal (FGA) performed for 30 minutes at 350 °C. This FGA step converts the surface functionalized oxide to a thin layer of GeO_2 resulting in improved electrical performance. 2.5 nm of HfO_2 was then deposited by ALD. 10 nm of RF sputtered TiN was deposited as the gate metal followed by low-temperature anneals in various ambients to tune the effective work function of the HfO_2/TiN gate stack.[4] A final FGA for 30 minutes at 350 °C completed device processing. These devices show excellent PMOS characteristics and will be discussed.

This work is supported by the SRC Global Research Corporation.

1 J.-S. Park, *et al.*, Appl. Phys. Lett. **90**, 052113 (2007).

2 J. Bai, *et al.*, Appl. Phys. Lett. **90**, 101902 (2007).

3 S. Swaminathan, *et al.*, J. Appl. Phys. **110**, 094105 (2011).

4 C. L. Hinkle, *et al.*, Appl. Phys. Lett. **100**, 153501, (2012).

3:40pm **EM+TF+OX+GR-MoA6 *In Situ* Infrared Spectroscopy Study on the Temperature Dependence on the Growth Mechanism of Atomic Layer Deposition of Al_2O_3 on InP(100)**, ***W. Cabrera***, The University of Texas at Dallas, *I.M. Povey*, Tyndall National Institute, *Y.J. Chabal*, The University of Texas at Dallas

One of the current challenges in fabricating III-V-based electronics is the growth of an interfacial layer during the atomic layer deposition (ALD) of high-k dielectrics on III-V substrates, which has led to poor quality electrical properties. A process that can mitigate this problem is the "clean-up" effect that occurs when trimethylaluminum (TMA) is deposited by atomic layer deposition during the formation of Al2O3. A recent theoretical study suggests that the principal pathway in the "clean-up" effect of TMA on the native oxides of GaAs and InGaAs involves oxygen gettering1. In this work, *in-situ* infrared absorption spectroscopy has been used to investigate the temperature dependence of the native oxide and the interface formation during Al2O3 deposition using TMA and deuterium oxide (D2O) on chemically-treated InP(100) surfaces. Upon annealing a degreased sample to 300°C, compositional changes are observed, as evidenced by new absorption features in the region of 900-1250 cm-1 of the infrared spectrum

prior to TMA exposure. The initial native oxide, comprised in part of In(PO3)3 is transformed into an InPO4-rich surface. Upon TMA exposure at 300°C, there is a clear loss of In(PO3)3 and gain of InPO4 (at 1007 and 1145 cm-1, respectively) along with the formation of Al-O bonds (absorption band at 800 cm-1)2. These observations are consistent with the "clean up" effect observed on GaAs3 and InGaAs4, and on InP(100)5 where TMA preferentially withdraws oxygen from the native oxide forming Al-O bonds. However, the TMA reduces In(PO3)3 and forsters the formation of InPO4. Furthermore, TMA exposure of the native oxide at lower deposition temperatures (150°C) gives rise to methoxy (CH3) formation as evidenced by the appearance of a band centered at 1475 cm-1. This indicates that TMA not only withdraws oxygen from the native oxide but also transfers a methyl group to the surface oxygen, which may lead to carbon contamination at the interface. Al2O3 oxide films are formed after 10 TMA and D2O cycles on both degreased native oxide and chemically treated (HF and (NH4)2S) InP(100) substrates, although the quality is higher on the (HF and (NH4)2S)-treated surface. A more clearly defined LO phonon mode is detected for that surface, suggesting that a denser oxide is formed.

1 S. Klejna et. al, *J. Phys. Chem. C*, **116**, (2012) 643-654

2 M. M. Frank et. al , *Appl. Phys. Lett.***82** (2003) 4758

3 C. L. Hinkle et. al, *Appl. Phys. Lett.,* **92** (2008) 071901

4 M. Milojevic,et. al *Appl. Phys. Lett.,* **93**, (2008) 202902

5 B. Brennan et. al, *Appl. Phys. Exp.,***4** (2011) 125701

4:00pm **EM+TF+OX+GR-MoA7 Ultimate Scaling of High-k Gate Dielectrics: Current Status and Challenges**, ***T. Ando***, *M.M. Frank, E.A. Cartier, B.P. Linder, J. Rozen,* IBM T.J. Watson Research Center*, K. Choi,* GLOBALFOUNDRIES*, V. Narayanan*, IBM T.J. Watson Research Center

INVITED

Current status and challenges of aggressive equivalent-oxide-thickness (EOT) scaling of high-k gate dielectrics via higher-k (>20) materials and interfacial layer (IL) scavenging techniques are reviewed [1]. La-based higher-k materials [2, 3] and La-silicate IL with HfO_2 [4] showed aggressive EOT values (0.5–0.8 nm), but with large effective workfunction (EWF) shifts toward the Si conduction band edge, limiting their application to nFET. Further exploration for pFET-compatible higher-k materials is needed. Meanwhile, IL scavenging is a promising approach to extend Hf-based high-k dielectrics to future nodes [4, 5]. Remote-scavenging techniques enable EOT scaling below 0.5 nm. We will review IL scavenging techniques from the viewpoints of (1) IL growth condition; (2) Choice of scavenging element; (3) Location of scavenging element; (4) Choice of high-κ material and (5) Maximum process temperature. Careful choice of materials and processes based on these considerations is indispensable. Mobility-EOT trends in the literature suggest that short-channel performance improvement is attainable with aggressive EOT scaling via IL scavenging or La-silicate formation. However, extreme IL scaling is accompanied with loss of EWF control [6] and with severe penalty in reliability [7]. Therefore, highly precise IL thickness control in an ultra-thin IL regime (<0.5 nm) will be the key technology to satisfy both performance and reliability requirements for future CMOS devices.

This work was performed by the Research alliance Teams at various IBM Research and Development Facilities.

[1] T. Ando, *Materials* **2012**, *5*, 478-500 [2] H. Arimura et al., *Electron Device Lett.* **2011**, 32, 288–290 [3] L. F. Edge et al., *Appl. Phys. Lett.* **2011**, 98, 122905 [4] T. Ando et al., *IEDM* 2009, 423-426 [5] L. Å. Ragnarsson et al., *IEDM* 2009, 663-666 [6] T. Ando et al., as discussed at *SISC* 2011 [7] E. A. Cartier et al., *IEDM* 2011, 18.4.1-18.4.4

4:40pm **EM+TF+OX+GR-MoA9 AR-XPS Study of Al_2O_3/In-based III-V Interfaces after Annealing under Vacuum at Low Temperature**, ***E. Martinez***, *H. Grampeix, O. Desplats,* CEA, LETI, MINATEC Campus, France*, A. Herrera-Gomez, O. Ceballos-Sanchez,* CINVESTAV-Unidad Queretaro, Mexico*, J. Guerrero, K. Yckache, F. Martin*, CEA, LETI, MINATEC Campus, France

III-V semiconductor substrates are a potential solution for MOSTETs down scaling below the 16 nm technological node. Indium based semiconductors, such as InGaAs, InAs and InP are promising compounds to improve the speed of operation. The quality of the interface between these high mobility substrates and the gate oxide is of crucial importance to preserve the devices electrical properties. Aluminium oxide is used to remove the As oxide ("self-cleaning" effect). The gate-last scheme is preferred to control of the high-k/III-V since it involves low temperature post deposition annealing [1]. State-of-the-art control of this interface has been obtained with annealing at 400°C under vacuum [2].In this work we focus on the impact of low temperature annealing under vacuum on the quality of the Al_2O_3/In-based III-V interfaces. We have studied the interfacial oxides formed between alumina and III-V substrates such as InGaAs, InAs and InP. Annealing at 600°C under ultra high vacuum (UHV) is first performed and compared to thermal treatments at 600°C and 400°C at 3 10^{-4} mbar. Substrate passivation is done with NH_4OH (4 %). The 3-nm thick alumina is deposited by Atomic Layer Deposition (ALD) using TMA and H_2O as precursor and oxidant. Angle-resolved photoelectron spectroscopy (AR-XPS) has been carried out to investigate the interfacial chemical bonding states. Consistent and robust analysis of the As 3*d*, P 2*p*, Ga3*d* and In 3*d* core levels was carried out through the simultaneous fitting method [3]. At 600°C, we show that, on InGaAs, no interfacial oxides are created after annealing under UHV, whereas a thin interfacial $InGaO_x$ is observed under secondary vacuum. A clear difference between the three substrates is observed after annealing at 400°C under 3 10^{-4} mbar. In particular, the indium oxidation and the relative stability of interfacial oxides are substrate dependant. On InAs, indium hydroxide is formed after annealing, by OH release from TMA/H_2O deposited alumina. This is not the case with additional elements such as Ga and P, which react with residual species to create their respective oxides. On InGaAs, a regrowth of $InGaO_x$ is observed after anneal, as a result of preferential oxidation of Ga. On InP, the $InPO_x$ interfacial oxide seems to decrease after anneal.**Acknowledgements**This work was performed with financial support from the MOS35 project funded by the French National Research Agency. Measurements were carried out at the NanoCharacterization Centre (NCC) of MINATEC. [1] H. Zhao et al., Appl. Phys. Let. 95, 253501 (2009)[2] Y. Urabe et al., Appl. Phys. Let. 97, 253502 (2010)[3] J. Muñoz-Flores et al., J. Electron. Spec. Rel. Phen. 182, 81 (2011)

5:00pm **EM+TF+OX+GR-MoA10 Effect of a H_2 Plasma Pre-treatment on the Reduction of Native Oxides at the PEALD Al_2O_3/InAs Interface**, ***E. Cleveland***, *L. Ruppalt, J.B. Boos, B. Bennett, J. Champlain, S.M. Prokes*, Naval Research Laboratory

The integration of high-*k* dielectrics with high mobility III-V semiconductor materials has attracted extensive interest recently as an alternative to Si-based complementary metal-oxide semiconductor (CMOS) applications at the 16 nm node and beyond. Among the III-V semiconductors, InAs is a promising material as the channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs) due to its extremely high electron mobility and high saturation velocity. However, problems arise in the fabrication of high performance channel MOSFETS due to the poor quality of the gate oxide/InAs interface. InAs has a highly reactive surface and on exposure to air will form a native oxide layer composed of In₂O₃ and As₂O₃. The complexity of these native oxides leads to the formation of a relatively high density of interface states which in turn act as charge traps thus pinning the Fermi level and degrading device performance. Wet-chemical treatments based on HCl and (NH4)2S have been found to be an effective means of removing these oxides, however, due to the rapid re-oxidation and lack of reproducibility a better means of interface cleaning is needed. Recently, there has been much interest in the field of surface cleaning combined with atomic layer deposition (ALD) in order to deposit high quality dielectrics on III-V semiconductor materials, such as InAs and GaSb. Therefore, we examined the use of a H₂ plasma as a means to obtain an oxide-free InAs interface prior to the deposition of high-*k* Al₂O₃ via plasma enhanced atomic layer deposition (PEALD). Ex-situ XPS, AFM, and C-V measurments were performed to establish the effect of the plasma exposure time, temperature and rf power on the removal of the native oxide. It will be demonstrated that by removing or reducing the native oxides on the InAs surface that the density of interface defects at the Al₂O₃/InAs interface can be reduced and enhance the electrical performance. Similar work done on GaSb will be discussed, where XPS spectra revealed a significant reduction in Sb-O features for longer H₂ plasma exposures as the peaks associated with Ga-O increased. C-V measurements of fabricated MOSCAPS also found that samples treated with longer H₂ plasma exposures exhibited better C-V characteristics.

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