Wednesday Afternoon, October 31, 2012

Electronic Materials and Processing
Room: 9 - Session EM+OX-WeA

Oxides and Dielectrics for Novel Devices and Ultra-dense Memory

Moderator: J.F. Conley, Oregon State University, J. Kim, The University of Texas at Dallas

2:00pm **EM+OX-WeA1 Dielectric Requirements for a Novel Tunnel-FET Based on Room-Temperature Superfluidity in Graphene Double Layers**, ***L.F. Register***, *X. Mau, D. Reddy, D. Basu, W. Jung, I. Sodeman, D. Pesin, A. Hassibi, A.H. MacDonald, S.K. Banerjee*, University of Texas at Austin **INVITED**

The Bilayer pseudo-spin Field Effect Transistor (BiSFET) is a novel transistor concept based on possible room temperature superfluidity in two graphene layers separated by a thin dielectric. In principle, the switching energy per device could be on the scale of 10 zJ, over two orders of magnitude below estimates for "end-of the roadmap" CMOS transistors. However, at the time of writing, neither a BiSFET nor just such room temperature superfluidity have been demonstrated, and doing so poses substantial challenges both theoretical and experimental. Most significant among these challenge for this novel device concept now appear to be those associated with its novel dielectric requirements. In this presentation I will cover the basic concepts behind graphene superfluidity and BiSFET concepts, our current understanding—and limits to that understanding—of the requirements for condensate formation, and how these requirements could impact BiSFET design. In particular, I will compare and contrast the dielectric needs for the proposed BiSFET to those of conventional transistors.

2:40pm **EM+OX-WeA3 Interfaces and Surfaces in Tunnel Field-effect Transistors**, ***G. Xing***, University of Notre Dame **INVITED**

Abstract: It is now recognized that compound semiconductor tunnel field-effect transistors (TFETs) can retain MOSFET-like speed at low supply voltages given that on-current and voltage can be lowered in proportion. To achieve high on-current at low Vdd, the staggered-gap and broken-gap AlGaSb/InAs heterojunctions and graphene are being developed. In this talk I will first outline the recent experimental progress in the development of interband tunnel transistors with sub-60 mV/decade subthrehold swing at Notre Dame. Subsequent discussions will be then focused on the impact of interfaces and surfaces of the transistor on the TFET performance, in particular, the interface between the gate dielectric and semiconductor as well as the semiconductor surface after transistor isolation etch.

4:00pm **EM+OX-WeA7 Resistive Switching Characteristics of Al_2O_3/TiO_2 Bilayer ReRAM dependent on Al_2O_3 Thickness**, ***H.Y. Jeon***, *J.S. Lee, J.G. Park, W.C. Jang, H.T. Jeon*, Hanyang University, Korea

The next generation nonvolatile memory (NGNVM) devices should satisfy the device properties such as high density, fast operation speed, low power consumption, and high reliability. Recently, many type-NGNVM candidates are extensively considered to replace the conventional nonvolatile memory devices; polymer random access memory (PoRAM), phase change random access memory (PRAM), spin transfer torque random access memory (STT-RAM), and resistive switching random access memory (ReRAM). Among the many type-NGNVMs, ReRAM has attracted a great deal of attention in semiconductor industry mainly due to its high density integration, long retention time, small cell size, and fast switching speed. Also, the ReRAM has the simple structure like metal/insulator/metal (MIM) structure allowing the fabrication of 3 dimensional stack and nano cross-bar structure. There are two types of resistive switching for ReRAM. One is unipolar resistive switching (URS) and the other is bipolar resistive switching (BRS). The URS means the operation of set (program) and reset (erase) are under the same polarity of bias, whereas the polarity of bias for set operation is opposite to that of bias for reset operation in the BRS. The URS type ReRAM needs current compliance to prevent hard breakdown of transition metal oxide (TMO) when measuring the resistive switching. The URS is usually observed in ReRAM using binary transition metal oxides such as NiO, TiO_2, and Al_2O_3, while the BRS appeared in ReRAM using perovskite materials like Cr:$SrZrO_3$, $Pr_{0.7}Ca_{0.3}MnO_3$. Among many deposition methods for metal oxide, atomic layer deposition (ALD) has recently received a great interest for manufacture of ReRAM. Especially, remote plasma ALD is expected to enhance the reactivity between metal-organic precursor and reactant gas with minimal plasma damage on substrate, allowing the low impurity content and high density of the deposited films. In RPALD, plasma is generated remotely outside of chamber. And the radicals and ions generated in plasma region enter into the chamber by a downstream flow for chemical reaction of deposition. In this study, we investigated URS switching behaviors of ReRAM using Al_2O_3/TiO_2 bilayer deposited by remote plasma atomic layer deposition (RPALD) method. The thickness of Al_2O_3 layers was varied to observe the discrepancy of set/reset voltage and operation current level. The deposited Al_2O_3 and TiO_2 films are perfectly amorphous structures and their binding states have nearly stoichiometric composition. When operating the ReRAM with different thickness ratio, the dependence of operation voltage and current level on the thickness of Al_2O_3 layers was observed.

4:20pm **EM+OX-WeA8 High- k $SrTiO_3$ Dielectric by Plasma-Assisted Atomic Layer Deposition**, ***N.Y. Garces***, *D.J. Meyer, B.P. Downey, V.D. Wheeler, D.W. Zapotok, C.R. Eddy, Jr.*, U.S. Naval Research Laboratory

Strontium titanate (STO) is a promising material that offers the possibility of achieving large dielectric permittivity (k) constants for gate dielectric and other applications. Thin (~28 nm) STO films were deposited by remote plasma-assisted atomic layer deposition on the native oxide of n-type Si substrates in an Oxford Instruments FlexAL reactor at ~250°C using Bis(Tris-IsopropylCyclopentadienyl) Strontium, Tetrakis(dimethylamido)titanium as metal precursors, and a remote oxygen plasma as oxidizer. The general approach to deposit the ternary perovskite SrTiO3 is by alternating the ALD of the constituents TiO2 and SrO in a specific ratio to control such properties as the stoichiometric composition and dielectric constant [1,2]. The deposition temperature was chosen to give optimum growth uniformity for both SrO and TiO2 and to avoid decomposition of the precursors. The growth rate of the STO films was ~ 0.14 nm/cycle, which is slightly higher than the combined growth rate of the individual components. Also, the STO growth rate and stoichiometry are highly dependent on the temperature of the strontium precursor.

Initial capacitance-voltage (C-V) and current-voltage (I-V) results on 50-250 µm diameter circular capacitors patterned on ALD SrO:TiO2 (1:1) films were obtained. These dielectrics exhibited a moderate (~ 20) dielectric constant with reduced reverse-biased leakage current of ~1.6x10-5 A/cm2but larger forward bias leakage current ~ 1.2x10-3 A/cm2at 1V. Hysteresis in forward and reverse C-V sweeps was not observed, suggesting that these films are high-quality with limited or no slow time-constant charge trapping. After annealing the STO films at 550ºC in N2 for 5 min, a reduction in the oxide thickness by ~ 9% was measured, as well as a small increase in the dielectric constant to ~ 28 as a result of crystallization [3].

During this study, the overall thickness of the dielectric was held relatively constant, while the relative ratio of SrO:TiO2 was varied to tune the stoichiometry of the films and to monitor changes in the dielectric constant, optical band gap, Eg, and the electrical performance of the resulting oxides. The thickness, g rowth rates, and ALD mode behavior of STO, SrO, and TiO2 oxides were evaluated by spectroscopic ellipsometry measurements. We will p resent electrical measurements of STO oxides of various compositions with optimized deposition conditions for the chosen precursors, as well as stoichiometry assessments by x-ray photoelectron spectroscopy.

1. Vehkamäki,et.al. Chem. Vap. Deposition, **7**, 75 (2001)

2. Popovici,et.al. *J. Electrochem. Soc.*, ***157***, *G1* (2009)

3. Langereis,et.al. *J. Electrochem. Soc.*, ***158***, *G34-G38* (2011)

4:40pm **EM+OX-WeA9 Micro-Antenna Coupled Nano-MIM Diodes: Modeling, Design, Processing and Application**, ***N. Goldsman***, Univ. of Maryland, CoolCAD Electronics LLC, *F. Yesilkoya,* Univ. of Maryland, *S. Potbhare,* CoolCAD Electronics, LLC, *M. Peckerar,* Univ. of Maryland, *A. Akturk,* CoolCAD Electronics, LLC, *K. Choi,* Univ. of Maryland, *W. Churaman,* U.S. Army Research Lab, *N.K. Dhar*, DARPA/MTO **INVITED**

An antenna coupled to a diode can convert electromagnetic power into DC power, which can be integrated over time and stored on a capacitor or used to charge a battery. The combination of the antenna and diode is typically called a "Rectenna". We are interested in developing a rectenna that operates in the infrared region of the electromagnetic spectrum. The applications of interest for IR rectennas include self-powering circuits and infrared imagers.

The rectenna structure we focus on consists of a micro-antenna and a rectifying metal-insulator-metal (MIM) diode for converting electromagnetic wave induced alternating current on the antenna to a direct current. The antenna couples to ambient or directed electromagnetic (EM) radiation, and the diode rectifies the AC signal for DC current and power generation. The frequency or the wavelength of the EM signal dictates the physical dimensions of the antenna, and the operating frequency of the

diode. Here one of the main challenges in achieving DC output upon IR radiation is to fabricate a diode capable of operating in the infrared range of frequencies, and more specifically at 30 Terahertz corresponding to 10 micrometer infrared radiation or approximately 300oK. To meet this challenge, we are fabricating metal-insulator-metal diode structures with oxide thicknesses of on the order a couple of nanometers or less.

An application of significant interest is a high resolution, high speed IR imager that can operate at room temperatures. Expanding from a single pixel to a complete large array is a challenge because the added complexity may give rise to electromagnetic coupling between adjacent elements, which needs to be accounted for. In addition, IR imaging, which corresponds to 30 terahertz region of operation, is special because it represents an 'in-between' region between radio and optical frequencies. At 10 micron wavelengths, the photons are typically too small in energy to economically convert their AC power into DC using semiconductor or quantum based photodetectors. At the same time, their frequency is too high to utilize standard PN or Schottky barrier diode based rectification. We thus explore the use of a micro-antenna coupled to a MIM diode for AC to DC conversion. A major difficulty here is to develop a diode that responds quickly enough to be forward biased during one part of the AC cycle and reverse biased to the other half of the cycle, without having the parasitic capacitance of the diode short out the signal. The rectenna we are developing uses a Nickel/Nickel-Oxide/Nickel (Ni-NiO-Ni) MIM structure, fabricated and designed using unique modeling and processing techniques.

5:20pm **EM+OX-WeA11 High-Electron-Mobility SiGe on Sapphire Substrate for Next Generation Ultrafast Chipsets**, ***H.J. Kim***, *Y. Park*, National Institute of Aerospace (NIA), *H.-B. Bae*, Korea Advanced Institute of Science and Technology, *S.H. Choi*, NASA Langley Research Center (NASA LaRC)

In the conventional silicon-on-sapphire (SOS) technology with the epitaxy of Si on *r*-plane (1-102) sapphire, typical device region do not need reverse bias between the substrate and device area for electrical separation, because SOS wafer is separated by the sapphire itself, a best insulator. The advantage is that the sapphire insulator is very thick, which engenders an ultra-small capacitance and therefore it can reduce parasitic capacitance and leakage current at a high operating frequency. However, SOS wafer has a limitation in carrier mobilities due to the silicon material. The mobilities of SiGe can be a few times higher than those of silicon due to the high carrier mobilities of germanium (p-type Si: 430 $cm^2/V{\cdot}s$, p-type Ge: 2200 $cm^2/V{\cdot}s$, n-type Si: 1300 $cm^2/V{\cdot}s$, n-type Ge: 3000 $cm^2/V{\cdot}s$ at 10^{16} per cm^3 doping density). Therefore, RF devices which are made with rhombohedral SiGe on c-plane sapphire can potentially run a few times faster than RF devices on SOS wafers.

NASA Langley's rhombohedral epitaxy uses an atomic alignment of the [111] direction of cubic SiGe on top of the [0001] direction of the sapphire basal plane (*c*-plane). It shows a sample of rhombohedrally grown SiGe on *c*-plane sapphire with a single crystalline percentage of 95%. Twin defects exist only at the edge of the wafer. The electron mobilities of the tested samples are between those of single crystal Si and Ge. For instance, the electron mobility of 95% single crystal SiGe is 1538 $cm^2/V{\cdot}s$ which is between 350 $cm^2/V{\cdot}s$ (Si) and 1550 $cm^2/V{\cdot}s$ (Ge) at $6x10^{17}$ $/cm^3$ doping concentration. Typically, a rhombohedral single crystal SiGe has 2 or 3 times higher carrier mobility than monocrystalline silicon. If the defects in SiGe can be removed, transistors with higher operational frequencies can be fabricated for a new generation of ultrafast chipsets.

5:40pm **EM+OX-WeA12 Fabrication and Characterization of Metal-Insulator-Insulator-Metal (MIIM) Tunnel Diodes**, ***A.N. Nasir***, *J.F. Conley*, Oregon State University

MIM tunnel diodes have been proposed for high speed applications such as hot electron transistors, IR detectors, and optical rectennas for IR energy harvesting as well as backplanes for LCDs. The majority of these applications require highly asymmetric and non-linear I-V behavior at low applied voltages. The standard approach to achieving asymmetric operation in MIM devices is through the use of metal electrodes with different workfunctions (Φ_M). However, the amount of asymmetry achievable using this method is limited by the Φ_M difference that can be obtained using practical metals. In this work, we use an alternative approach to achieving asymmetric and non-linear operation – engineering of the insulating tunnel barrier using nanolaminate pairs of insulators with different bandgaps and band-offsets to produce asymmetric tunnel barriers. Electrons tunneling from one metal electrode to the other will see a different shape barrier depending on the direction of tunneling and the bias applied.

Recently, we found that atomic scale roughness at the bottom metal-insulator interface can dominate the I-V characteristics of MIM diodes, even overwhelming the influence of Φ_M difference. By using the amorphous metal ZrCuAlNi (ZCAN) as an ultra-smooth bottom electrode in combination with high quality dielectrics deposited via ALD, we were able to fabricate MIM diodes dominated by FN tunneling. In this work, nanolaminate insulator stacks consisting of either HfO_2/Al_2O_3, Ta_2O_5/Al_2O_3,ZrO_2/Al_2O_3, or HfO_2/ZrO_2 are deposited on sputtered ZCAN bottom electrodes via ALD. Al dots form the top gate electrode.

MIIM I-V characteristics were found to be sensitive to the relative thickness as well as the arrangement of the individual dielectric layers. In the ZCAN / Al_2O_3 / HfO_2 / Al orientation, the asymmetric tunnel barrier opposes the effect of the asymmetric Φ_M, a larger current is measured at positive bias, and asymmetry is lower than for a neat Al_2O_3 insulator device. However, in the ZCAN / HfO_2 / Al_2O_3 / Al orientation, the asymmetric tunnel barrier enhances the asymmetric Φ_M, a larger current is measured at negative bias, and asymmetry is greater than for neat Al_2O_3 or HfO_2 insulator devices. High asymmetry is seen when conduction in both dielectric layers is dominated by FN tunneling rather than bulk limited mechanisms. Ta_2O_5/Al_2O_3, e.g., did not show an enhancement in asymmetry.

In conclusion, we have fabricated dual insulator MIIM diodes that exhibit improved asymmetry over single layer MIM diodes. These results represent an advancement of the understanding necessary to engineer thin film based MIM tunnel devices for microelectronics applications.

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