Wednesday Morning, October 20, 2010

Thin Film
Room: Dona Ana - Session TF+EM-WeM

High K Dielectrics for Si Electronics
Moderator: S. Gupta, University of Alabama

8:00am **TF+EM-WeM1 Moore's Law - From Simple Scaling to Integrating New Materials and Introducing New Device Architectures**, ***R. Hendel***, Periodic Structures Inc. **INVITED**

Moore's Law has been the driver for semiconductor integrated circuits over more than 40 years. Relentless scaling of dimensions switching provided increasing functionality and performance, resulting in leading edge single chips today that incorporate more than 1 Billion transistors.

All attempts on predicting the end of Moore's Law have been futile – innovations have always allowed continued scaling at reduced cost. However, while Moore's Law appears to be a continuous curve, we rarely reflect on the underlying changes that had to occur to enable this rate of progress. These changes comprised device architecture, the introduction of new materials and break-through processes.

Since Moore's Law describes a learning curve for which cost reduction is central, process simplicity frequently won out over performance advantages if the latter came at high cost. Self-aligned implanted poly-gate over the early metal gate structures is a prime example. Aggressive reduction in the cost per function also provided performance benefits: Smaller transistors switched faster and used less power to do so – truly a win-win situation.

Key innovations along this path were:

· The switch from thermal diffusion doping to implant

· The introduction of CMP, which was key in increasing the number of metal layers that could be integrated.

· The introduction of high-k dielectrics in conjunction with metal gates which addressed the critical gate leakage problem and will allow the introduction of new and better performing channel materials.

Compared to the past, the future will require even more innovation along three potential directions:

· Continuous improvements of current methodologies along existing technologies, consisting of solid engineering and hard work.

Innovations pursued in this category are: highly regular layouts, new channel materials in conjunction with modified hi-k/MG (yet planar) structures.

· Significant changes to traditional device structures and processes.

An example of innovations pursued in this category is the FinFET, which presents significant challenges in materials and processes that must be resolved before introduction into the manufacturing cycle.

· Radical new structures and approaches resulting in major deviation from today's mainstream technologies.

An example is new fundamental circuit components such as the Memristor or new approaches available if considering device operations at cryogenic temperatures (which may be feasible for server farms), allowing the exploration of concepts such as superinsulators.

This presentation will highlight the state-of-the-art in process technology and discuss challenges that require attention and timely solutions.

8:40am **TF+EM-WeM3 Non-destructive Depth Profiles of Hafnium Silicate Films by Angle-Resolved and Variable-Kinetic Energy XPS**, ***C. Weiland***, *N. Lorenz, R. Opila*, University of Delaware

High dielectric constant, or high-k films are currently being employed in semiconductor devices. Hafnium silicate ($Hf_xSi_{(1-x)}O_2$) films are a promising material system for such applications, as they combine the high dielectric constant of HfO_2 with the high stability against crystallization of SiO_2. The $Hf_xSi_{(1-x)}O_2$/Si interface must be defect free as defects at this interface can create charge centers which decrease channel mobility. Atomic layer deposition (ALD) is frequently used to deposit high-k films, and provides excellent thickness control and conformality by reacting only one saturating layer of reactant at a time. This work focuses on studying the composition and interface quality of $Hf_xSi_{(1-x)}O_2$ films deposited by ALD using novel silicon precursors and water as the oxidizer. Films are analyzed using non-destructive depth profiles by angle-resolved and variable-kinetic energy X-ray photoelectron spectroscopy (ARXPS, VKE-XPS). In ARXPS, the effective probe depth is varied by changing the takeoff angle between surface and detector. As a complementary technique, VKE-XPS provides depth profiles by adjusting the incident X-ray energy, and thus the corresponding inelastic mean free path of the photoemitted electrons. VKE-XPS also allows the ability to probe deeper into films than conventional lab-based sources, providing the possibility of analyzing thicker films or entire gate stacks. Using these techniques, we have studied the composition and interface quality of $Hf_xSi_{(1-x)}O_2$ films deposited using various Si precursors. The presence of charge at the interface manifests itself as shifts in the energy of the photoelectron peaks. Using this data, we can determine charge at the high-k/silicon interface as well as measure band offsets.

9:20am **TF+EM-WeM5 Study of SiO_2 and SiN_x Passivation of HfInZnO Oxide Semiconductor Thin Film Transistor**, ***J.C. Lee***, *E.H. Lee, J.G. Chung, B. Anass, J.H. Lee, J.S. Park, M.K. Ryu*, Samsung Advanced Institute of Technology, Korea

ZnO based oxide semiconductor is a promising material for thin film transistor which has transparent, high electric mobility, and the advantage of low temperature process. Several kinds of ZnO based oxide semiconductors (InZnO, GaInZnO, HfInZnO, etc.) have been adapted to the active material of thin film transistor. However most of ZnO based oxide semiconductors have very sensitive property to ambient environment. It is essential to prevent the penetration of moisture into ZnO based oxide thin film transistor (TFT). In the purpose of preventing moisture penetration and/or protecting damage from TFT processes, SiN_x or SiO_2 passivation layer is used frequently.

In this study, we investigated the interface reactions between amorphous HfInZnO (Hf:In:Zn= 10:35:55, 40nm thickness) oxide semiconductor active layer and the passivation layer of SiN_x or SiO_2 (20 nm thickness). TEM, XPS and SIMS were used to investigate the interface reactions such as atomic diffusion, reduction of HfInZnO, chemical state, microstructure.

According to experimental results, a SiO_2 phase and Indium metallic state were observed at the interface between SiNx and HfInZnO active layer. On the other hand, there was not observed Indium metallic state at the interfaces between SiO_2 and HaInZnO layers. In the case of SiN_x passivation, it is considered that some Si took oxygen from Indium oxide in HfInZnO and oxidized to SiO_2. And some of Indium oxide reduced to metallic Indium at the interface. Indium diffusions from HfInZnO layers into passivation layers were observed at the both of SiNx and SiO_2 samples. In the case of SiN_x passivation, it was a little bit higher diffusion than that of SiO_2 passivation. The low binding energy shift was observed at the Zn_{2p} XPS spectra at the both samples. However, there was no distinct difference at the Hf_{4d} spectra.

If there is metallic Indium between passivation and HfInZnO active layers, the metallic Indium may influence the conductance of active layer. The threshold voltage (V_{th}) shift of thin film transistor (TFT) could be affected by the change of conductance of active layer.

We observed that the V_{th} negative shift of the TFT used SiN_x passivation was higher than that of SiO_2 passivation. It may be due to the existence of metallic Indium at the interface.

In this report, it will be described the relationships between interface reactions and the property of HfInZnO oxide TFT in detail.

9:40am **TF+EM-WeM6** , ***E.J. Bersch***, *M. Di*, University at Albany, *S.A. Consiglio, R.D. Clark, G.J. Leusink*, Tokyo Electron America Inc., *A.C. Diebold*, University at Albany

There has been much attention paid recently to the lowering of the threshold voltage (V_t) that is accomplished by including an additional ultrathin (~5-10 Å) oxide layer in the high-k/metal gate metal oxide semiconductor field effect transistor (MOSFET) gate stack. We have investigated the TiN/HfO_2/La_2O_3/SiO_2/p-Si stack, where the La_2O_3 layer is the so-called V_t-shift layer. For several variations of this stack, where both the thickness and the position of the La_2O_3 layer were systematically varied, we measured two quantities directly related to the V_t, the flatband voltage (V_{fb}) and the Si band bending. The V_{fb} was measured using capacitance-voltage (C-V) measurements on stacks with 500 Å TiN layers, and the Si band bending was measured on sister wafers with 30 Å TiN layers. For a set of samples where the thickness of the La_2O_3 between the HfO_2 and SiO_2 layers was varied, we observed that the V_{fb} and Si band bending both become more negative as the thickness of the La_2O_3 was increased. For a set of samples where position of the La_2O_3 within the HfO_2 layer was varied, we observed that the V_{fb} and Si band bending became less negative as the amount of HfO_2 between the La_2O_3 and the SiO_2 was increased. These observations support the proposition that there is a dipole at the La_2O_3/SiO_2 interface which affects the Si band bending, as has been reported in the literature.[1,2] We have also observed that there is a difference in the V_{fb} and Si band bending in TiN/HfO_2/La_2O_3/SiO_2/p-Si stacks with thermally grown and chemically grown SiO_2 layers. Results of this study as well as one where the

thickness of thermally grown SiO_2 layers was varied will be presented, and it implications on the theory of the interface dipole with be discussed.

1. K. Kita, et al., *Appl. Phys. Lett*, 94, 132902 (2009).

2. P.D. Kirsch, et al., *Appl. Phys. Lett*., 92, 092901 (2008).

10:40am **TF+EM-WeM9 Modification of Defect-State Concentrations with Vacuum Ultraviolet and Ultraviolet Irradiation of Hafnium-Oxide Dielectric Layers**, ***H. Ren***, University of Wisconsin-Madison, *S.-L. Cheng, Y. Nishi,* Stanford University, *J.L. Shohet,* University of Wisconsin-Madison

The effects of 7.2 eV vacuum ultraviolet (VUV) and 4.9 eV ultraviolet (UV) irradiation on a 20 nm HfO2 layer atomic layer deposited (ALD) on (100) Si substrate are explored with electron-spin resonance (ESR). Silicon dangling-bond defect concentrations (*Pb* centers) and positively charged oxygen vacancies (*E*' centers) were measured with *g*-factor fitting. The concentrations of the defect states are presented. VUV irradiation increases the level of *Pb0* and *Pb1* states, while UV decreases the level of *Pb0* and *Pb1* states, but increases the level of *E*' states significantly. [i] [#_edn1] In addition, rapid thermal annealing (RTA) mitigates the effects of both VUV and UV irradiation. Surface-potential measurements with a Kelvin probe show that electron photoemission process dominate VUV irradiation. On the other hand, electrons are transferred from *E*' states to the silicon substrate during UV irradiation. At the same time, electrons are photo-injected into the dielectric layer from the substrate. Furthermore, VUV spectroscopy measurements show that the Fermi level for *E*' defect states is around 4.7 eV, which is within the bandgap of the dielectric layer. Also, previous work [ii] [#_edn2] shows that the E' states, as oxygen-interstitial defects (OID), are located within the HfO2 layer. We conclude that VUV irradiation modifies the concentrations of the silicon dangling-bond defect states and UV irradiation can be a potential source for positively charge oxygen vacancies during the processing.

Work Supported by the Semiconductor Research Corporation under contract 2008-KJ-1781

[i] [#_ednref] H. Ren, S.L. Cheng, Y. Nishi and J.L. Shohet, *Applied Physics Letters* (to be published)

[ii] [#_ednref][ii] J.L. Lauer, J.L. Shohet and Y.Nishi, *Applied Physics Letters* **94**, 162907 (2009)

11:00am **TF+EM-WeM10 Plasma Enhanced Atomic Layer Deposition of Ruthenium Ultra-Thin Films for Advanced Metallization**, ***J. Swerts***, *S. Armini, L. Carbonell, D.A. Annelies, F.A. Alexis, S. Mertens, T. Witters, M. Schaekers, Z. Tökei, G. Beyer*, IMEC, Belgium, *V. Gravey, A. Cockburn, K. Shah, J. Aubuchon,* Applied Materials Inc., *S. Van Elshocht*, IMEC, Belgium

Electrochemical deposition of Cu for interconnect metallization traditionally uses Physical Vapor Deposition (PVD) of a Cu seed layer on top of a PVD Ta/TaN barrier to conduct the current. However, the limitations of PVD in respect of step coverage compromise its use in future technology nodes. Atomic Layer Deposition (ALD) for barrier deposition combined with seedless Cu electroplating is one of the metallization routes explored for sub-25 nm line widths. However, compatibility with seedless electroplating seriously limits the choice of materials. Among the different candidates, Ru-based layers have been identified as very promising.

We report the growth and scalability of Ru films by plasma-enhanced ALD (PE-ALD) from MethylCyclopentadienylPyrrolylRuthenium (MeCpPyRu) and N_2/NH_3 plasma. The layers were deposited using a 300 mm showerhead type reactor (AMAT) with direct plasma capability. The substrate temperature during deposition was 330C. The Ru growth per cycle was 0.04 nm. As substrates we used Si wafers with 100-300 nm SiO_2 on which a thin TaN or TiN layer was deposited by ALD or PVD.

The metal nitride is needed as a growth enabler since Rutherford backscattering spectrometry (RBS) showed that only 1E14 Ru atoms/cm^2, i.e. less than a monolayer, were deposited on SiO_2 after 120 PE-ALD cycles. The minimal thickness of the metal nitride to enable Ru growth has been determined to be as low as 0.7-0.8 nm which is promising for scaling. Growth studies on scaled and thick ALD TiN or TaN still showed a limited growth inhibition during the first 40 cycles followed by a linear growth behavior. Static time-of-flight secondary ion mass spectroscopy (TOFSIMS) suggests Ru layer closure for a film thickness around 2 nm.

Atomic force microscopy revealed that the root mean square roughness values were below 0.4 nm for film thicknesses up to 20 nm. X-ray diffraction showed that the Ru layers have a hexagonal structure. The density of the Ru layer was 11.75 g/cm^3 as derived from X-ray reflectivity and RBS. Elastic recoil detection analysis and TOFSIMS indicate that the N, O, C-levels in the bulk Ru layers were << 1%. Surface analysis by static TOFSIMS showed the presence of organic contamination identified as MeCp ligands from the Ru precursor. In contrast, the Pyrrolyl ligand was not observed. A post deposition thermal treatment of the Ru film removes the ligand organic contamination. The impact of this surface contamination on the seedless Cu electroplating efficiency will be discussed. Finally, the step coverage of TiN/Ru and TaN/Ru stacks in narrow lines (65-15 nm width) was evaluated by transmission electron microscopy.

11:20am **TF+EM-WeM11 Effects of Hydrogen Plasma Pretreatment on Superconformal Gap-Filling of Cu-Al Alloy**, ***H.K. Moon***, *N.-E. Lee*, Sungkyunkwan University, Republic of Korea

As the feature of microelectronic interconnects has continued to shrink, Cu resistivity is expected to increase at the nanoscale due to increased surface and grain boundary scattering of electrons. To prevent increase of the resistivity in nanoscale interconnects, alloying Cu with other metal elements such as Al, Mn, and Ag is being considered to increase the mean free path of the drifting electrons. The formation of Al alloy with a slight amount of Cu broadly studied in the past. The investigation of Cu alloy with a very small Al fraction, by contrast, recently started. The formation of Cu-Al alloy is limited in wet chemical bath and was mainly conducted for fundamental studies by sputtering or evaporation system. However, these deposition methods have a limitation in production environment due to poor step coverage in nanoscale Cu metallization. In this work, gap-filling of Cu-Al alloy was conducted by cyclic MOCVD (metal organic chemical vapor deposition), followed by thermal annealing for alloying, which prevented an unwanted chemical reaction between Cu and Al precursors and hydrogen in the gas phase. To fill the Cu-Al alloy into sub-100nm trench without overhang and void formation, furthermore, hydrogen plasma pretreatment of the trench pattern with Ru barrier layer was introduced in order to suppress of Cu nucleation and growth near the entrance area of the nano-scale trench by minimizing adsorption of metal precursors. As a result, superconformal gap-fill of Cu-Al alloy could be achieved successfully in the 40-nm trench with an aspect ratio of 4. Examined morphology, microstructure, chemical composition, and electrical properties of superfilled Cu-Al alloy will be discussed in detail.

11:40am **TF+EM-WeM12 Depth Resolved Cathodoluminescence Spectroscopy of Amorphous High-*k* Dielectric $LaLuO_3$**, ***S. Shen***, Ohio State University, *Y. Liu, R.G. Gordon,* Harvard University, *L.J. Brillson*, Ohio State University

We have used depth-resolved cathodoluminescence spectroscopy (DRCLS) to measure the native point defects and reaction-induced defects within ultrathin $LaLuO_3$ dielectric films. The rare earth oxide $LaLuO_3$ is gaining much attention because of its high dielectric constant (28 ~ 32) and its potential application to replace SiO2 as a gate dielectric for Si microelectronics, requiring both sub-nanometer thick gate oxide layers and low leakage currents. $LaLuO_3$ deposited by atomic layer deposition (ALD) provides films with high crystallization temperature and relatively high conduction band offset, but they have non-negligible leakage currents that are attributed to electronic trap states in the band gap. Annealing can partially reduce these traps but can also induce diffusion/reaction at the $LaLuO_3$ interfaces. We used DRCLS to determine the changes in defect levels of WN/20 nm $LaLuO_3$/Si gate structures as a function of annealing and the introduction of an Al_2O_3 diffusion barrier at the Si interface. A 10 nm WN/20nm $LaLuO_3$/Si structure as-grown exhibits defect emissions at 2.4, 3.2, 3.8, 4.2 and 4.7 eV as well as a 5.48 eV band gap. With 300ºC cyclic annealing, 10 nm WN/20nm $LaLuO_3$/Si, the band gap emission is absent and high energy emissions at 4.2 and 4.7 eV shift to 3.8 eV. A 10 nm WN/20nm $LaLuO_3$/0.4 nm Al_2O_3/Si interlayer structure exhibits negligible difference from the interlayer-free stack without anneal. However, with annealing, the WN/20nm $LaLuO_3$/0.4 nm Al_2O_3/Si defects at high energy and the band gap remain unchanged while the lower energy defects are suppressed. The 5.48 eV band gap emission agrees with an internal photoemission gap of 5.3 eV measured previously. The 4.2 and 4.7 eV emissions are consistent with weighted density function approximation calculations showing two oxygen-vacancy-related states at similar energies near the $LaLuO_3$ conduction band edge. The DRCLS–measured degradation of optical features with annealing of the interlayer-free structure is attributed to Si diffusion and reaction with $LaLuO_3$ as observed by cross sectional TEM. This degradation is suppressed with the Al_2O_3 barrier layer. Furthermore, the annealing of the interlayer structure reduces all the low energy defect emissions. Finally, the highest lying state at 4.7 eV above the valence band (0.78 eV below the conduction band) agrees reasonably well with the 0.6-0.7 eV electrical measurements of leakage current. These results highlight the importance of annealing with a diffusion barrier at the Si interface to suppress defects within $LaLuO_3$ without Si reaction at the $LaLuO_3$ interface.

Authors Index

Bold page numbers indicate the presenter