Tuesday Morning, October 19, 2010

Plasma Science and Technology
Room: Aztec - Session PS1-TuM

Advanced FEOL Etching II

Moderator: A. Agarwal, Applied Materials Inc.

8:20am **PS1-TuM2 Sidewall Polymer Management of sub 20nm Shallow Isolation Trench (STI) Etch via Pulsed Plasma**, ***X. Hua***, *X. Ji, J. He, J.H. Choi, A. Khan*, Applied Materials Inc.

The thickness of sidewall polymer accumulated on feature is typically a few nanometers during plasma etching. How to manage this thin polymer layer becomes critical to successful pattern transfer by plasma etch, because it equals >10% of the actual feature size as semiconductor devices are aggressively scaled down below 20nm. The impact of this thin layer on conductance of species in the features is not negligible any more when feature size is shrunk below 20nm, especially in high aspect ratio applications. To make minimum depth loadings, i.e. intro cell/micro loadings, and ideal feature profiles are extremely challenging and strongly dependent on how we manage this sidewall polymer. In this wok, we will discuss how we can utilize pulsed plasmas to manage this polymer layer. Since the residence times of typical plasma etch conditions are in order of ms~s and the period of pulsed plasma is ~ms, species has extra time to move into or out of the feature when it is the off cycle, as compared conventional plasma sources of continuous wave mode. This unique property of pulsed plasma leads to 1) thinner polymer coverage (less redeposition, radicals moving out of the feature) or 2) thicker polymer accumulation (more deposition, radicals moving into the feature from the gas phase), depending on plasma conditions. Better introcell/ micro loadings, more rounded/less pinch off trench bottom are demonstrated by using low duty cycle (<60%) pulsed plasmas than continuous wave plasmas. The influence of duty cycles/frequency of the pulsed plasmas on feature profile, depth loading was investigated in details. In synchronized pulsed plasmas, continuous tapered trench profile is demonstrated with no pinchoff bottom. With optimized duty cycle ratio between source and bias powers, microloading is achieved below 5% of etch depth (>300nm). Pulsed plasma has shown enormous advantage over conventional continuous wave plasma source to control the pattern transfer of future semiconductor fabrications.

8:40am **PS1-TuM3 Feature Scale Model of Shallow Trench Isolation (STI) Etch in HBr Plasma and Comparison with Experiments**, ***S. Sriraman***, *T. Panagopoulos, A. Paterson, H. Singh, V. Vahedi*, Lam Research Corporation

Continued scaling in the semiconductor industry provides new challenges for critical etch applications in front-end logic and memory devices. As device sizes shrink, control of Shallow Trench Isolation (STI) features to create active area islands become more important. Typical logic STI performance metrics for a 300mm wafer include trench angle, trench depth and iso-dense depth loading and their corresponding within-wafer uniformity. In addition to these metrics, memory STI application includes a challenging requirement for intra-cell depth loading that arises due to within-feature variation of the space critical dimensions (CD) in the dense feature array. These stringent profile control requirements are typically met by operating halogen-based Transformer Coupled Plasma (TCP™) in the mid-pressure operating regime.

This paper will discuss the semi-empirical feature scale model of STI etch in HBr plasma to address iso-dense and intra-cell trench depth loading for an etch stack representative of memory STI features. Plasma diagnostics and reactor-level models are implemented to characterize the HBr plasma produced in the TCP configuration process chamber. Kinetic parameters in the model are constrained by matching simulated feature profiles with those experimentally obtained at various process conditions that are a subset of the process space of interest. The feature scale model is quantitatively calibrated to the experimental profiles and validated for prediction within the process space. The validated profile simulator is used to identify reactor-level process knobs that minimize iso-dense and intra-cell depth loading. The advantages of calibrated process-specific profile simulation in enabling efficient exploration of parameter space during process development and future challenges facing STI trench depth etch will be discussed.

9:00am **PS1-TuM4 Synchronous Plasma Pulsing For Etch Applications**, ***M. Haass****, *M. Darnon, E. Pargon, C. Petit-Etienne, L. Vallier, P. Bodart, G. Cunge*, CNRS-LTM, France, *S. Banna, T. Lill*, Applied Materials Inc., *O. Joubert*, CNRS-LTM, France

Plasma processes have been used for many years in the manufacturing of semiconductors. They have been so far the only technological solution to address the critical dimension control at the nanometer range imposed by the continuous downscaling of the CMOS devices dimensions.

However, the current etch processes are reaching their limits of controlling the etch selectivity and the critical dimensions at the atomic scale. In this study we investigate the potential of pulsed plasmas to further improve dry etching processes.

The experiments are carried out in a commercially available 300 mm AdvantEdgeTM tool from Applied Materials Inc. The inductively coupled plasma is sustained by two RF generators operating at 13.56 MHz, one to generate the plasma and the other mainly to polarize the wafer. These generators have been modified using the PulsyncTM system to allow pulsing at frequencies between 10 Hz and 20 kHz and duty cycles between 10 and 90 %. Even though a delay can be applied between the generators only the synchronous case is studied here. Several modifications of the plasma chamber were carried out in order to use advanced plasma diagnostics like in situ ellipsometry, UV absorption spectroscopy and mass spectroscopy. Furthermore an angle resolved XPS system is connected to the plasma chamber under vacuum allowing quasi in-situ analysis of the wafer surface after etching.

This article focuses on HBr/O2 plasmas dedicated to STI (Shallow Trench Isolation) etch processes. We demonstrate the ability of synchronously pulsed etch plasmas at different frequencies and duty cycles to modify the etched profiles strongly compared to the standard continuous case. Especially experiments carried out at a frequency of 1 kHz and a duty cycle of 20 % show a very distinct alteration. In this case, ellipsometry measurements indicate a sharp increase in time compensated etch rate (etch rate relative to the actual plasma ON time of the etch process). Additionally, the etched profiles show a strongly enhanced quality, in particular a high selectivity, uniformity and a minimization of the aspect ratio dependent etching phenomena. We demonstrate that these improvements are linked to the balance between plasma dissociation and recombination during the ON and OFF time of the pulsed plasma which can directly influence the composition of neutral and ion flux. This balance is controlled by the duty cycle rather than the pulsing frequency.

9:20am **PS1-TuM5 Characterization of Pulsed Plasma Etch Reactors with an Integrated Global Plasma-Feature Scale Model**, ***A. Balakrishna***, *A. Agarwal, P. Stout, S. Rauf, K. Collins*, Applied Materials Inc.

9:40am **PS1-TuM6 Atomic Layer Etching of Graphene using O_2 Radical and Ar Neutral Beam**, ***W.S. Lim***, *Y.Y. Kim, G.Y. Yeom*, Sungkyunkwan University, Republic of Korea

Graphene is a two-dimensional hexagonal lattice of carbon atoms with the thickness of one or a few atomic layers. Due to its material stability and strength, absence of defects, and unique electronic band-structure, graphene holds considerable promise for a number of applications in nanoscale electronics, optoelectronics, and mechanics in addition to showing fundamental interest in condensed matter physics. Many potential applications, such as graphene-based high-speed field-effect transistors, require graphene to be patterned to the nanoscale and, in some cases, graphene needs to be etched precisely with atomic layer precision. However, through the conventional reactive ion etching, it is difficult to control the etch depth precisely due to the fluctuation of the etch process in addition to the damage to the graphene by the reactive ions.

In this study, to overcome the above problems, the atomic layer etching technique (ALET) has been applied in the etching of graphene, and the etch characteristics of graphene by ALET were investigated. For the adsorption gas, O_2 was used, and Ar neutral beam was used for the desorption of the adsorbed compound. For the few layer graphene deposited on the SiO_2 (300 nm)/ Si substrate, the monolayer etching condition of graphene was observed by supplying O_2 radical at a pressure higher than the critical pressure during the adsorption step and by supplying an Ar beam at a dose

***** Coburn & Winters Student Award Finalist

higher than the critical dose. Self-limited etching of graphene could be obtained using O_2 radical ALET.

10:40am **PS1-TuM9 Etching of Magnetic Stack for Development of Thermally-assisted Magnetic Access Random Memory**, ***J. Pereira***, *X. Mellhaoui*, LTM - UMR 5129 CNRS, France, *J. Shin*, Crocus Technology, France, *E. Pargon*, LTM - UMR 5129 CNRS, France, *J. Reid*, Crocus Technology, France, *O. Joubert*, LTM - UMR 5129 CNRS, France

11:00am **PS1-TuM10 III-V Etch Challenges for Beyond 20nm Node**, ***U. Shah***, *B. Turkot, M. Radosavljevic, M. Shaw, S. Clendenning, B. Chu-Kung*, Intel Corp.

The scaling of CMOS transistors to 20nm and beyond may invoke utilization of materials that are far different in electrical and mechanical properties from conventional silicon. InGaAs, InP, GaAs are examples of such materials being considered for future device fabrication and as such will present numerous challenges for etch. These include balancing profile needs against stringent selectivity and scalability requirements to address the myriad of device needs at this node. Etch characterization of these materials using various processing chemistries (Cl2, CH4, H2), tool conditions (chuck temperature, power, bias, pressure) and tool types, as well as a variety of material stacks has been carried out using 3-4" wafers. GaAs and InGaAs etch rates of ~40-45A/s at high chuck temperature of 225 degrees are obtained for 30nm lines spaced at 1-50um. A linear relationship between etch rate and temperature is also observed with H2/Cl2 chemistry. Chuck temperature impact on trench/ line profiles is understood on the basis of volatility of the byproducts as well as on the nature of the resulting sidewall passivation. Data showing the difficulties in pitch scaling and controlling etch rates of stacked materials will also be discussed.

Authors Index

Bold page numbers indicate the presenter