Plasma Science and Technology
Room: Aztec - Session PS-MoM

Advanced BEOL / Interconnect Etching I

Moderator: K. Kumar, TEL Technology Center America

8:20am **PS-MoM1 Plasma Processes Challenges for Porous SiOCH Patterning in Advanced Interconnects**, ***N. Posseme***, CEA-LETI-MINATEC, France, *T. Chevolleau,* CNRS-LTM, France, *T. David,* CEA-LETI-MINATEC, France, *M. Darnon,* CNRS-LTM, France, *F. Bailly, R. Bouyssou, J. Ducote, C. Verove,* STMicroelectronics, France, *O. Joubert*, CNRS-LTM, France **INVITED**

The choice of copper/Low-k interconnects architecture is one of the keys for integrated circuits performances, process manufacturability and scalability. Today, the implementation of porous low-k material becomes mandatory in order to minimize the signal propagation delay in the interconnections. In this context, the traditional plasma processes issues (the plasma-induced damages, dimension and profile control, selectivity) and new emerging challenges (sidewalls surface roughness, dielectric wiggling) become the critical points to control the reliability and defectivity.

Based on plasma-surface interaction understanding, the main issues and also the potential solutions will be illustrated through different process architecture using metallic or organic hard masks strategies.

9:00am **PS-MoM3 TiN Selectivity Improvement by DC Voltage Effect in a DC+ Dual Frequency Capacitive Coupled Plasma Etcher**, ***M. Nishino***, *M. Honda, Y. Ooya, R. Shimizu*, Tokyo Electron AT Limited, Japan

Metal Hard Mask(TiN) damascene scheme has been chosen by many logic semiconductor manufacturers for 2x or beyond BEOL processes. Due to issues related to Aspect Ratio, wiggling, and integration with low mechanical stress resistant porous low-k dielectric materials, TiN hard mask has become thinner and less resistant to etch. As the technology node decreases to sub 20nm, Self-Aligned Via(SAV) process will be introduced for MHM dual damascene scheme to maintain Via CD within the confined specifications of the MHM. With this scheme, TiN MHM is exposed to RIE etch twice: once during partial via formation and another in trench etch. Due to such tight process margins, many semiconductor manufacturing companies are focusing on high selective chemistry for TiN during both Via and Trench dielectric etch process. The DC+ Dual frequency etcher is a capacitive coupled plasma etcher with a superimposed DC voltage. This configuration has been proven to be more effective for maintaining TiN hard mask during dielectric etching. A negative DC bias is applied to the upper Si electrode. The Si electrode surface reacts with CFx radicals from fluorocarbon based plasma and the fluorine component of bulk plasma was reduced. This phenomenon is the interaction between fluorocarbon based plasma and Si electrode which was induced by DC voltage. This paper presents an investigation of TiN hard mask high selective process from this interaction. We measured Ne and Vdc areas of MHM trench process both with and without DC voltage conditions and investigated the direction of Ne/Vdc windows as MHM trench process at first . We evaluated this interaction effect from Ne and Vdc trend with DC voltage and observed that DC voltage did not only acquire higher TiN selectivity to dielectric (maintain TiN thickness) but also reduce TiN HM facet etching rate (control CD shift) in dielectric etching. This is one of the advantages for the DC+ Dual frequency capacitive coupled plasma etcher .

9:20am **PS-MoM4 RIE Process Challenges in sub 30nm node Trench First Metal Hard Mask Scheme**, *K. Zin,* ***Y. Feurprier***, *Y. Chiba, H. Kida,* Tokyo Electron Limited, *M. Ishikawa,* Toshiba America Electronic Components, *Y. Mignot,* STMicroelectronics, *Y. Yin*, IBM Systems and Technology Group

As scaling of microelectronic devices approaches sub 30nm nodes, many material and module process challenges in BEOL plasma patterning have been reported. One of the methods that has gained traction over recent years for enabling sub 20nm feature patterning is the Trench First metal Hard Mask (TFmHM) scheme. While this scheme solves or mitigates many challenges that are inherent with Via First Trench Last (VFTL) Scheme, it introduced other dielectric RIE process and hardware challenges. One of the root causes of the former is the fact that all patterns and materials are exposed to plasma at the same time. As such, the simultaneous control of via, trench and chamfer profiles (i.e. Critical Dimensions, depth, taper profile, etc), the need to control selectivity between multiple patterning layer (TiN, TEOS, ULK, Barrier cap, etc), and ULK damage control has become more pertinent in the dielectric etch. As the direct result of such tight process guidelines, the hardware challenges arise and new dimensions in process controls are needed. The prolonged exposure of the TiN to the plasma created the need for more robust production worthy hardware. The required selectivity of the materials necessitate temperature controllable chucks. The more complex patterning techniques require ULK preservation and other uniformity controls. In this paper, the RIE efforts on process controls of the profiles, material selectivity, associated hardware challenges and possible future roadmaps under TFmHM scheme will be discussed.

This work was performed by the Research team at TEL Technology Center America in joint development with IBM Research Alliance Teams in Albany, NY.

9:40am **PS-MoM5 BEOL Double Patterning: Challenges for Etch**, ***Y. Yin***, *J.C. Arnold, M. Colburn, S. Burns, S. Holmes, C. Koay,* IBM Systems and Technology Group, *R. Kim,* Global Foundries, *G. Landie,* STMicroelectronics, *D. Horak,* IBM Systems and Technology Group, *Y. Mignot,* STMicroelectronics, *H. Tomizawa*, Toshiba Corporation

As feature critical dimension (CD) shrinks towards and beyond the 22nm node, limitations of traditional patterning processes become critical. Conventional 193nm immersion lithography is not able to resolve trenches below 40nm half pitch with a single exposure. Patterning vias at appropriate CD and spacing is equally challenging. Extreme ultraviolet (EUV) lithography offers appropriate k1 reduction to solve these problems, but the equipment and metrology infrastructure is not in place to support 15nm node development on a large scale. Thus, much of the industry's attention is being paid to double patterning techniques based on existing 193nm imaging capability. In this paper, we will discuss various double patterning schemes and the associated technical challenges for plasma etching - both for generating patterns with sub-40nm half pitch and for utilizing the resultant masking stacks for BEOL etching. In particular, we will review the issues associated with applying "double-exposure double-etch" sequences, "double-exposure single-etch" approaches, and sidewall image transfer to formation of dual-damascene structures in advanced ultra low-k dielectrics.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

10:40am **PS-MoM8 Film Diffusivity-Dependent Role of VUV/O_2 and Ar^+ Ions in SiCOH Ultra-low-*k* Dielectric Films**, ***J. Lee***, *D.B. Graves*, University of California, Berkeley

The degradation of porous ultra-low-*k* material, like SiCOH, under plasma processing continues to be a problem in the next generation of integrated-circuit fabrication. Due to exposure with many species during plasma treatment, such as photons, ions, radicals, etc., it is difficult to identify the mechanisms responsible for plasma-induced damage. Some studies have attempted to decouple plasma-generated species in order to study the effect of individual components and possible synergistic effects [1,2]. Using a vacuum beam apparatus with a calibrated VUV lamp and Ar ion gun, we show that 147 nm VUV photons and the presence of molecular O2 cause a loss of methylated species in SiCOH, creating a silica-like structure on the upper layer of the exposed material. The extent of the VUV/O2 induced damage as well as the effect of Ar ion bombardment is dependent on the interconnectivity, and thus diffusivity, of the material. In highly interconnected material, Ar+ bombardment may seal pores, restricting O2 diffusion into the film and reducing damage compared to VUV/O2 alone. The effects of vacuum beam exposures are shown to be comparable to plasma exposures under 'plasma cure' (no energetic ion bombardment) and some rf-biased conditions. Using Fourier-transform infrared (FTIR) spectroscopy and mercury probe measurements, we show that VUV/O2 exposure causes loss of carbon, resulting in a hydrophilic, damaged layer that is susceptible to H2O absorption, which leads to an increased dielectric constant. These results suggest that both VUV photons and high-energy ions can play important roles in the generation of plasma-induced damage.

[1] Jinnai B, Nozawa T, Samukawa S 2008 *J.Vac. Sci. Technol.* B **26** 1926.

[2] Uchida S *et al.* 2008 *J. Appl. Phys.* **103** 073303

11:00am **PS-MoM9 Oxygen Containing Photoresist Ashing Chemistries with Less Damage to Low-k Films**, ***R. Gupta***, *N. Stafford, C. Dussarrat, V. Omarjee*, Air Liquide

Oxygen-based plasma has been traditionally used for ashing patterned photoresist on low dielectric SiCOH (low-k) thin films. During the ashing process, energetic plasma species remove carbon (or CH3 group) from the exposed regions of the low-k film causing an increase in the dielectric constant of the film. The modified low-k film is also susceptible to water absorption which leads to higher dielectric constant and a degraded performance of the patterned device structure (such as collapsing and loss of critical dimensions) [1,2]. Moreover, higher porosity films will be

required in future to achieve even lower dielectric constant and these films will be even more susceptible to plasma damage. Therefore, there was a need for new ashing chemistries to reduce the level of damage to the porous low-k film. A systematic study was performed with mixtures of O2 and selected molecules such as the standard CO2, CH4 or newly thought ashing chemistries. The ashing performance of the selected gas mixtures was compared with pure O2 for a similar thickness of resist removal. In order to highlight the chemistry effects of gas mixtures, the ashing was performed in similar conditions (i.e. RF power, temperature and pressure) as used for pure O2using a CCP RIE chamber.

A parametric study completed with pure O2 indicates that an increase in RF power and pressure generally leads to an increase in low-k damage. However, flow rate change with constant pressure did not show significant modification in damage characteristics. Damage to low-k film is improved by using gas mixture of the new chemistries and O2. The Hg-probe dielectric measurements reveal a least increase in dielectric constant with this mixture. Dilute Hydrofluoric (HF) acid tests also reveal the higher etch resistance of low-k films ashed with this mixture. Auger/XPS depth profile metrology is used to obtain elemental profiles of the damaged low-k films. In addition, residual gas analyzer data is being reviewed to understand better the etch gas chemistry to correlate to the damaging behavior of selected chemistries.

References:

Lee et al., Thin Solid Films, 517, (2009)

Zhou et al. AVS 2009. http://www.avsusergroups.org/pag_pdfs/2009_6zhou.pdf .

11:20am **PS-MoM10 Ultra-low k Integration Challenges and Plasma Etch Solutions For 22nm Node**, ***Y. Zhou***, *Z. Cui, J. Pender, S. Nemani, M. Naik*, Applied Materials Inc.

Higher porosity and new film chemistry are required to drive down k value of porous ultra low k (ULK) dielectrics integrated in advanced BEOL stacks. The challenge of integrating ULK dielectrics is compounded by shrinking dimensions. Taking a tri-layer resist via-first-trench-last integration scheme as an example, as the technology nodes progress, lower k value dielectrics are more prone to ashing damage. The resulting damaged layer accounts for a larger percentage of remaining film, resulting in higher integrated k value. Therefore, ashing improvement achieved for earlier nodes is not sufficient for the 22nm node. A particular ULK integration challenge is via to line spacing. The tight pitches at 22nm leave little tolerance for enlargement of the via size and shape. Previously acceptable levels of profile bowing can now directly lead to shorting. In this work, the challenges of ashing damage and via profile bowing are examined with a via first trench last integration scheme. It is identified that ashing is responsible for the majority of via profile bowing, and the key to reducing via bowing and ashing damage is to improve the ashing selectivity of organic mask to dielectrics. Different approaches are taken to improve ashing selectivity, including the traditional ashing chemistry/plasma optimization and a new pre-ash dielectric passivation scheme. These optimizations have significantly improved both physical and electrical performance.

11:40am **PS-MoM11 Highly Selective Etching of SiOCH over SiC Films by Dual Frequency CCP with DC Bias Superimposed to Upper Electrode**, ***T. Yamaguchi***, *K. Takeda,* Nagoya University, Japan, *C. Koshimizu,* Tokyo Electron AT Limited, Japan, *H. Kondo, K. Ishikawa, M. Sekine, M. Hori*, Nagoya University, Japan

The dual frequency capacitively coupled plasma (CCP) with negative DC bias superimposed to the upper electrode has been proposed to realize high performance etching technologies. Denpoh *et al.* have discussed a mechanism under the DC bias superimposition that secondary electrons generated at the upper electrode transport through a bulk Ar plasma to the counter electrode. Kawamura *et al.* have also discussed about effects of the secondary electrons and a characteristic of the superimposed DC/RF sheath. Since the fluorocarbon (CF) etching plasma with the DC bias has not ever analyzed, we have measured various parameters and discuss the effect of the DC bias on the selective etching of SiOCH over SiC.

We used a CCP reactor for 300 mm wafer. VHF (60 MHz) power and DC bias were simultaneously applied to the upper electrode. RF (13.56 MHz) power was applied to the lower electrode where the samples were placed for etching experiments. A mixture gas of Ar, N_2 and C_4F_8 introduced with flow rates of 800, 100, and 10 sccm, respectively. Pressure was kept at 5.3 Pa.

Bulk plasma parameters such as electron density and CFx densities were measured when the DC bias changed. The electron density was 1.3×10^{11} cm^{-3} without the DC bias. In contrast, with the bias of -1200V, that gained up to 2.1×10^{11} cm^{-3}. This increase can be interpreted that positive ions accelerated by the DC bias bombarded the upper electrode with higher energy and then generated and supply more secondary electrons to the bulk plasma.

Notably, CF_2 radical density was decreased from 2.5 to 1.5×10^{13} cm^{-3} with the DC bias. It is well known that the bulk density depends on the surface loss probability, α, of the CF_2 radical. The α gained by dangling bonds creation by the ion bombardments. As the result, we believed that more fluorine-rich compounds in bulk plasma were lost by the adsorption and reaction on the reactive surfaces. In fact, with the DC bias of -1200V, SiOCH/SiC selectivity was improved significantly to 68 from 5.5without the DC biasing. This improvement was mainly brought by the etch rate decreasing SiC from 18.5 to 1.3 nm/min while the etch rate of the SiOCH film was maintained almost constant.

Surface analysis results showed that CF polymerized layer was not grew thicker on the SiOCH by such chemical reactions as $C + O \rightarrow CO$, $C + N + H \rightarrow HCN$. However, in the SiC case, a polymerized layer was relatively thicker because removal reactions were suppressed by lack of F-rich compound. Consequently, the highly selective etching for SiOCH/SiC films was achieved by differentiating the polymerized layer formation.

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