Plasma Science and Technology
Room: Galisteo - Session PS+MN-WeM

Plasma Processing for 3D Integration, TSV, and MEMS
Moderator: M. Darnon, CNRS-LTM, France

8:00am **PS+MN-WeM1 High Etch Rate of TSV using by Ultra Self-Confined VHF-CCP**, ***Y. Morikawa***, *M. Yoshii, N. Mizutani, K. Suu*, ULVAC, Inc., Japan

Thru silicon via (TSV) etch process for deep and high-aspect ratio structure has been studied thoroughly for applications such as MEMS devices. Recently, TSV used in 3D-LSI devices, the via diameter and depth would be several tens of microns, and, the package for CMOS image sensors using TSV may have via diameters and depths up to 100 microns. A diameter of above 50um account for 50 % of TSVs. Therefore, development of high etch rate about 50um via is very important for realizing these applications. In this study, a large via size of 50 um etching in a low-pressure process was focused by using very high frequency capacitive coupled plasma (VHF –CCP) with an ultra self-confined system. This plasma system is simple parallel plate CCP. And the cathode has a structure designed to minimize the stray capacitance (Cs) and impedance (L) to get a low-pressure process of about 100Pa or more. Low-pressure process was carried out on the plasma confined, because mean free pass is very short. And, ion energy distribution (IED) is also controllable by low-presser process with VHF bias. The bimodal IED changes under low-pressure. The peak of high-energy side is reduced, and a charge exchange peak appears. It is considered that the charge exchange is important to anisotropic Si etching with VHF bias. Finally, an etch rate of more than 60 μm/min was realized. It was found that the Si etch rate depended on fluorine radical density and ion energy distribution, so, the high rate was obtained by creating a high fluorine radical density condition by using a high pressure condition of 100Pa using a VHF-CCP reactor with an ultra confined system and SF6 gas chemistry.

8:20am **PS+MN-WeM2 Very Uniform and High Rate TSV Etching Process in Advanced NLD Plasma**, *Y. Morikawa*, ***T. Murayama***, *K. Suu*, ULVAC, Inc., Japan

The h igh-density of thru silicon via (TSV) is indispensable to the utilization and improvement in performance of 3D-LSI. Advanced high aspect ratio TSV etching technologies are required for high-density TSV formation. We have developed a new etching system for TSV application. This s ystem is a planer type magnetic neutral loop discharge (NLD) plasma, which is named as advanced NLD. For high rate silicone etching, it is very important to understand not only the high density of the plasma generation but also the high density of fluorine atoms . In this study, a novel RF antenna ' M ulti Stacked rf A ntenna' has also been developed for the purpose of high rate etching. This antenna consists of multistage spiral turn rf antennas to reduce self- inductance (L), and is increased from turn of spiral to extend the inductive coupling discharge region. T he L feature of this antenna is 0. 95 uH and it is a low L antenna compared to the standard spiral antenna (1.7uH) . As a result of performing the electron density measurement of the NLD plasma using this MS antenna, it succeeded in the high-density plasma production of $1x10^{12}$ / cm^3 by the process pressure of 7 Pa. Next, the Si etching process development was performed using the a dvanced NLD etcher. Si etching characteristics employing advanced NLD plasma were studied with respect to distance from an antenna. As a result, the etching rate improved 4 times more compared to the standard NLD. Finally, the diameter of 1 .5 um was attained by the anisotropic etching of 8. 5 um/min, and the aspect ratio is 5.3 using the a dvanced NLD etcher.

8:40am **PS+MN-WeM3 Deep Reactive Ion Etch Process Optimization for Control of Sidewall Profile and Morphology as a Function of Aspect Ratio**, ***R.J. Shul***, *R.L. Jarecki, T.M. Bauer,* Sandia National Laboratories*, M. Wiwi*, LMATA Government Services

Deep reactive ion etching (DRIE) has become an enabling technology for the fabrication of many integrated microsystems, including accelerometers and gyroscopes, micro-fluidic devices, sensors, electrostatically actuated devices, and devices requiring back side optical access. The ability to etch deep Si structures with anisotropic sidewalls hundreds of microns deep has established a new set of devices in the MEMS area. Significant improvements in equipment and understanding of the process conditions have improved device yield and performance, and process reliability. Even with these improvements, several process issues are not well understood and often limit applications for the process. For example, sidewall morphology is often dominated by scalloping created by the iterative deposition-depassivation-etch cycle. Scalloping may make it difficult for deposition of materials on the sidewalls post DRIE or create non-optimal flow conditions for micro-fluidic devices. In addition, profile control of deep structures as a function of aspect ratio has not been optimized. For example, we have observed that creating positively tapered trench sidewalls often results in a trench bottom that exhibits a characteristic micromasked, grassy appearance. Conversely, eliminating the grass often results in a profile that undercuts the etch mask. Depending on the application, these phenomenon prevent the use of DRIE for device fabrication or cause the process to be optimized for specific structures thus preventing yield of other structures. In this presentation, we report on our efforts to vary DRIE process conditions to optimize sidewall profile and sidewall morphology as a function of aspect ratio. Structures considered in this study range from 10 microns to 700 microns in width, with etch depths to several hundred microns. We observe that passivation time, as well as ion energy, and ion flux in both the depassivation and etch cycles, have significant effect on the sidewall profile as a function of aspect ratio. We have also included morphing experiments in this study, where morphing is changing DRIE process parameters as a function of total process time. To optimize sidewall profile and morphology, the magnitude of the process changes during the morphing process is not necessarily linear with time. Results of these experiments will also be reported.

Sandia National Laboratories is a multi program laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

9:00am **PS+MN-WeM4 XeF_2 Vapor Phase Silicon Etch used in the Fabrication of Movable SOI Structures**, ***J. Stevens***, *R.J. Shul,* Sandia National Laboratories*, M. Wiwi, C.L. Ford,* LMATA Government Services*, T. Plut, T.M. Bauer*, Sandia National Laboratories

Vapor phase XeF_2 has been used in the fabrication of various types of devices including MEMS, resonators, RF switches, and micro-fluidics, and for wafer level packaging. In this presentation we demonstrate the use of XeF_2 Si etch in conjunction with deep reactive ion etch (DRIE) to release single crystal Si structures on Silicon On Insulator (SOI) wafers. XeF_2 vapor phase etching is conducive to the release of movable SOI structures due to the isotropy of the etch, the high etch selectivity to silicon dioxide (SiO_2) and fluorocarbon (FC) polymer etch masks, and the ability to undercut large structures at high rates. Also, since XeF_2 etching is a vapor phase process, stiction problems often associated with wet chemical release processes are avoided. Monolithic single crystal Si features were fabricated by etching continuous trenches in the device layer of an SOI wafer using a DRIE process optimized to stop on the buried SiO_2. The buried SiO_2 was then etched to handle Si using an anisotropic plasma etch process. The sidewalls of the device Si features were then protected with a conformal passivation layer of either FC polymer or SiO_2. FC polymer was deposited from C_4F_8 gas precursor in an inductively coupled plasma reactor, and SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD). A relatively high ion energy, directional reactive ion etch (RIE) plasma was used to remove the passivation film on surfaces normal to the direction of the ions while leaving the sidewall passivation intact. After the bottom of the trench was cleared to the underlying Si handle wafer, XeF_2 was used to isotropically etch the handle Si, thus undercutting and releasing the features patterned in the device Si layer. The released device Si structures were not etched by the XeF_2 due to protection from the top SiO_2 mask, sidewall passivation, and the buried SiO_2 layer. Optimization of the XeF_2 process and the sidewall passivation layers will be discussed. The advantages of releasing SOI devices with XeF_2 include avoiding stiction, maintaining the integrity of the buried SiO_2, and simplifying the fabrication flow for thermally actuated devices. Sandia National Laboratories is a multi program laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

9:20am **PS+MN-WeM5 $SF_6/O_2/HBr$ Plasma Processes for the Etching of High Aspect Ratio through Silicon Via**, ***S. Avertin,*** STMicroelectronics, France*, E. Pargon, T. Chevolleau,* Ltm - Umr 5129 Cnrs, France*, F. Leverd, P. Gouraud, C. Verove,* STMicroelectronics, France*, O. Joubert*, Ltm - Umr 5129 Cnrs, France

Today, the integration density and the chip dynamic power consumption are limiting and restricting phenomena. More than 50% of this consumption is due to long horizontal interconnects, and this rate is projected to increase. One solution to resolve these problems is 3D-Integration which provides smaller wire-length distribution by minimizing the connection length thanks to the fabrication of vertical vias through the silicon substrate or/and the chip. The ITRS roadmap requirement is to etch vias with 2-5 μm in

diameter and high aspect ratio (>5). For deep silicon etching, the Bosch etch process which consists in alternating isotropic etching and deposition steps leads to the formation of the so-called scalloping phenomenon on the sidewalls (>100nm). In this paper, we propose to characterize and develop conventional plasma etching processes as an alternative to the Bosh process. The etching development is carried out in ICP reactor accepting 300mm wafers (DPSII from AMAT^{TM}) using SF_6/O_2/HBr plasma chemistries. The scientific objectives are to study the etching mechanism and passivation layer formation in order to get high etch rate (>3µm.min^{-1}), straight profiles and a controlled undercut (<50nm). The etching profiles and etch rates have been analysed using Scanning Electron Microscopy while etch and passivation mechanisms have been studied by quasi-in-situ X-ray Photoelectron Spectroscopy (XPS) and plasma diagnostics (Mass Spectroscopy, ion flux probe..). Preliminary results indicate that the etch mechanisms are strongly driven by the ratio of neutral over ion fluxes and that the etch process is very sensitive to microscopic effects such as the local loading of fluorine and oxygen radicals which is directly correlated to the local pattern density. Through a better understanding of the etch mechanisms, high aspect ratio silicon via with anisotropic profiles and minimized undercut have been obtained.

9:40am **PS+MN-WeM6 Study on the High Aspect Ratio Si Etch for D2x Devices**, ***Y. Gwangyong**, P. Jongchul*, Samsung Electronics, Republic of Korea

As the design rule of the semiconductor devices decreases, the device fabrication technology is facing many difficulties. One of issues is the STI trench etching profile in case of the aspect ratio(A/R) over 20, and the traditional etching technology is not working properly any more. One among those problems is intra-cell loading which is due to the insufficient exhaustion of by-product from the narrow space (less than 30nm). The other is the bowing profile which results in the bad STI filling to generate the severe electrical short fails of a DRAM device. In this study, we researched and developed the innovative STI trench etching technologies to improve those problems. The one is the bias-pulsed plasma etching that repeats periodically plasma ON and OFF, which gave the dramatic decrease of the intra-cell loading. In addition that gave the side p assivation effect to result in straight side-slope without bowing. These two effects are due to the byproduct exhaustion and the radical attaching during the plasma OFF time. A nd the high temperature etching process and the multi-step Oxygen flashing process also improved the intra-cell loading significantly. We got to know that these new Si etching technologies are successfully applied to the future high A/R(> 15:1) STI process for D2x DRAM devices.

10:40am **PS+MN-WeM9 Key Challenges in Extremely High-Aspect-Ratio Dielectrics Etching at 3x nm DRAM and Beyond**, ***S.K. Lee**, J.-H. Sun, S.O. Lee, J.-S. Bang, S.-I. Lee, C.-M. Lim, S.-Y. Kim, D.-G. Lim, S.-K. Park, J.-G. Jung*, HYNIX Semiconductor Inc., Republic of Korea

One of key issues in fabricating the dynamic random access memories (DRAM) is to control the vertical profile effectively during the etching of a SiO2 high aspect ratio contact holes (HARC). In order to ensure acceptable Cs (>25fF/Cell) for DRAM at half pitch (HP) 3x nm and beyond generation, it is required of fabricating cell capacitors having very highly aspect ratio above 50:1. Thus, the HARC etching technology to get smaller bowing width as well as larger opening area becomes the most difficult challenges among numerous DRAM fabrication steps. This is because of trade-off between both bowing and opening requirement during HARC etching. Although the mechanism of bowing and not-opening has reported in several studies at above 70nm technology nodes, still has not yet been reported at hp 3x nm and beyond. In this presentation, especially, we will focused on the HARC etching issues at Nitride Fence supported Capacitor (NFC) scheme which is used to prevent leaning. Capping is arose by several factors, which reduce the etch rates and cause the contact opening failure, then eventually affects on the electrical characteristics. The types of capping studied in this work can be divided into three categories as the etching proceeded, such as polymer pinch-off, excess polymer capping originating from polymer rich chemistry at top region, and non-steady polymer deposition and removal at etch front. In this study, we investigated that capping issues become more serious when 2MHz range power is added to increase contact opening margin. To avoid these types of different failures aforementioned, it is necessary to understand the plasma etching behavior at hp 3x nm and beyond compared to previous technology nodes. In addition, beyond typical bowing position, an additional bowing position at NFC is also key concern issues within oxide layer between hard mask (HM) and Nitride from the wafer top surface. This is caused by the ions scattered from the mask side-wall slope on the contact-hole. It can be reduced effectively by adjusting HM material, thickness, and etching conditions. Especially, HARC etching parameters also play an important role to suppress the bowing and capping. We will report here how contact hole's opening and bowing are enhanced, and how they can be controlled by adjusting etching conditions also. It is suggested that optimizing the etching condition with a suitable concept in this work would be the most effective solution during the HARC etching process. Consequently, Key approaches on HARC etch processes for fabricating of a contact hole in SiO2 with aspect ratios of 50:1 and beyond were evaluated in this work in detail.

11:00am **PS+MN-WeM10 Microstructures Etching on Silicon with the STiGer Process**, ***T. Tillocher**,* GREMI, France*, J. Ladroue,* GREMI - STMicroelectronics, France*, F. Moro, G. Gommé, P. Lefaucheux,* GREMI, France*, M. Boufnichel,* STMicroelectronics, France*, P. Ranson, R. Dussart*, GREMI, France

Authors Index

Bold page numbers indicate the presenter

— A —

Avertin, S.: PS+MN-WeM5, **1**

— B —

Bang, J.-S.: PS+MN-WeM9, 2
Bauer, T.M.: PS+MN-WeM3, 1; PS+MN-WeM4, 1
Boufnichel, M.: PS+MN-WeM10, 2

— C —

Chevolleau, T.: PS+MN-WeM5, 1

— D —

Dussart, R.: PS+MN-WeM10, 2

— F —

Ford, C.L.: PS+MN-WeM4, 1

— G —

Gommé, G.: PS+MN-WeM10, 2
Gouraud, P.: PS+MN-WeM5, 1
Gwangyong, Y.: PS+MN-WeM6, **2**

— J —

Jarecki, R.L.: PS+MN-WeM3, 1
Jongchul, P.: PS+MN-WeM6, 2
Joubert, O.: PS+MN-WeM5, 1
Jung, J.-G.: PS+MN-WeM9, 2

— K —

Kim, S.-Y.: PS+MN-WeM9, 2

— L —

Ladroue, J.: PS+MN-WeM10, 2
Lee, S.-I.: PS+MN-WeM9, 2
Lee, S.K.: PS+MN-WeM9, **2**
Lee, S.O.: PS+MN-WeM9, 2
Lefaucheux, P.: PS+MN-WeM10, 2
Leverd, F.: PS+MN-WeM5, 1
Lim, C.-M.: PS+MN-WeM9, 2
Lim, D.-G.: PS+MN-WeM9, 2

— M —

Mizutani, N.: PS+MN-WeM1, 1
Morikawa, Y.: PS+MN-WeM1, **1**; PS+MN-WeM2, 1
Moro, F.: PS+MN-WeM10, 2
Murayama, T.: PS+MN-WeM2, **1**

— P —

Pargon, E.: PS+MN-WeM5, 1
Park, S.-K.: PS+MN-WeM9, 2
Plut, T.: PS+MN-WeM4, 1

— R —

Ranson, P.: PS+MN-WeM10, 2

— S —

Shul, R.J.: PS+MN-WeM3, **1**; PS+MN-WeM4, 1
Stevens, J.: PS+MN-WeM4, **1**
Sun, J.-H.: PS+MN-WeM9, 2
Suu, K.: PS+MN-WeM1, 1; PS+MN-WeM2, 1

— T —

Tillocher, T.: PS+MN-WeM10, **2**

— V —

Verove, C.: PS+MN-WeM5, 1

— W —

Wiwi, M.: PS+MN-WeM3, 1; PS+MN-WeM4, 1

— Y —

Yoshii, M.: PS+MN-WeM1, 1