Wednesday Afternoon, October 20, 2010

Graphene Focus Topic Room: Brazos - Session GR+MS-WeA

Low Dimensional Carbon Device Manufacturing Moderator: A.C. Diebold, The University at Albany-SUNY

2:00pm GR+MS-WeA1 Material Properties of Epitaxial Graphene in RF Devices, D.K. Gaskill, U.S. Naval Research Laboratory, J.S. Moon, HRL Laboratories, LLC, G.G. Jernigan, J.C. Culbertson, J.L. Tedesco, U.S. Naval Research Laboratory, J. Robinson, The Pennsylvania State University, P.M. Campbell, N. Garces, V.D. Wheeler, J.K. Hite, R.L. Myers-Ward, C.R. Eddy, Jr., A.L. Friedman, U.S. Naval Research Laboratory, M. Fanton, The Pennsylvania State University INVITED The advent of the world's first epitaxial graphene (EG) RF field effect transistors (FETs), grown on semi-insulating SiC wafers, has generated tremendous interest in the electronics community since devices can be fabricated using conventional photolithographic approaches [1]. Recently, RF FETs have shown an f_{max} of 14 GHz at 5 V_{ds} for a 2 μm gate width and better results are expected as gate widths are scaled down. To push the performance metrics for wafer-scale EG FETs significantly higher, key materials issues must be addressed. Some of these issues are morphology and thickness control, enhanced mobility, uniformity of sheet carrier density and resistivity, and substrate defects. Here we describe NRL-HRL-Penn State approach in the DARPA CERA program for forming EG via Si sublimation from SiC wafers and the impact of material issues on RF device performance will be discussed.

Epitaxial graphene was synthesized using an Aixtron VP508 reactor on the Si- and C-faces of 4H- and 6H-SiC semi-insulating 0° oriented substrates from 1225 to 1700°C and for 10 to 300 min. Samples were 50.8 and 76.2 mm wafers and 16 x 16 mm² witnesses. Both *in-vacuo* (10⁻⁶ to 10⁻⁴ mbar) and Ar ambient (50-200 mbar) sublimation conditions were investigated. Growth conditions resulted in continuous EG on Si-face witnesses < 1 nm thick as measured by atomic force microscopy, x-ray photoelectron spectroscopy and Raman spectroscopy, whereas growth on C-face witnesses could be varied, depending upon growth conditions, from island formation to continuous sheets > 10 nm thick. Using the witness samples, 300 K mobilities over 2,100 and 27,000 cm²V⁻¹s⁻¹ were found for 10x10 µm² sized Hall patterns for EG on the Si- and C-face of SiC, respectively.

The growth of EG on 50.8 mm Si-face *wafers* resulted in excellent relative resistivity uniformity of 2.8% and 300 K Hall mobilities up to 2,700 cm²V⁻¹s⁻¹ were found. Raman spectroscopy mapping of the 2D peak on the wafers determined: (1) the majority of the film was monolayer, (2) two layers of EG could be found at step edges and (3) EG was continuous across the wafer. RF FETs exhibited state-of-the-art ambipolar behavior such as electron field-effect mobility of 6,000 cm²V⁻¹s⁻¹ with I_{on}/I_{off} ratio of 19 and peak transconductance of 600 mS mm⁻¹ per 1 fF µm⁻² gate oxide capacitance. The f_T•L_g performance metric of 10 GHz•µm was established. Additionally, we will discuss our recent work on EG growth on 76.2 mm wafers as well as the impact of morphological features and Ar ambient controlled graphenization on future RF devices.

Supported by DARPA CERA (N66001-08-C-2048) and ONR.

[1] J.S.Moon *et al.*, IEEE Electron Dev Lett **31**, 260 (2010)

2:40pm GR+MS-WeA3 In situ Growth, Microscopy, and Spectroscopy of Graphene Films, J. Hannon, IBM T.J. Watson Research Center INVITED

I will describe *in situ* low-energy electron microscopy (LEEM) studies of graphene synthesis on SiC and polycrystalline Ni substrates. Using spatially-resolved electron diffraction (LEED-IV), we have determined the atomic structure, layer thickness, and stacking sequence of individual graphene domains with sub-micron precision. Using spatially-resolved electron energy loss spectroscopy (EELS), we have correlated the local electronic and atomic structure. I will discuss how these measurements aid in interpreting transport measurements from these same samples. This work was performed in collaboration with Ruud Tromp.

4:00pm GR+MS-WeA7 High-frequency Transistors from Wafer-scale Epitaxial Graphene, Y.-M. Lin, IBM T.J. Watson Research Center INVITED

Graphene has generated enormous research interest because of its unique physical and electronic properties. In particular, a large part of the research interests and activities arise from the high intrinsic carrier mobility and saturation velocity in graphene that may lead to higher-frequency electronic devices/circuits than can be achieved by conventional semiconductor materials. Here we present the top-gated graphene transistors fabricated on two-inch graphene wafer.

Graphene was epitaxially grown on the Si face of a high-purity semiinsulating SiC 4H(0001) wafer by thermal decomposition, yielding a film of 1-2 layers of graphene over the entire wafer. The as-grown graphene film possesses an electron (*n*-type) carrier density of ~ 3x1012 cm-2 and a Halleffect mobility between 1000–1500 cm2/V.s. In order to preserve the intrinsic mobility of graphene in the top-gated device structure, an interfacial polymer layer was spin-coated on the graphene prior to the oxide deposition. The carrier mobility of top-gated Hall bar devices varied between 900-1520 cm2/V.s across the two-inch wafer, indicating that little degradation in graphene mobility.

The cutoff frequency *f*T is obtained from the high-frequency S-parameters measurements, which signifies the highest frequency at which a transistor can propagate an electrical signal. For a gate length of 550 nm, the measured *f*T ranges between 20 to 53 GHz. For a shorter gate length of 240 nm, *fT* as high as 100 GHz was measured. This 100 GHz cutoff frequency is the highest speed achieved to date for any type of graphene devices, including exfoliated and CVD -grown graphene. Further enhancement in the device performance is expected to be achieved by continued improvements in the electrical characteristics of epitaxial graphene and the gate length scaling.

*In collaboration with K. Jenkins, D. Farmer, C. Dimitrakopoulos, H.-Y. Chiu, A. Valdes-Garcia, A. Grill, and P. Avouris.

4:40pm GR+MS-WeA9 Graphene-on-SiC and Graphene-on-Si MOSFETs on 75 mm Wafers, J.S. Moon, D. Curtis, M. Hu, S. Bui, D. Wheeler, T. Marshall, HRL Laboratories, LLC, D.K. Gaskill, P.M. Campbell, Naval Research Laboratory, P. Asbeck, University of California at San Diego, G.G. Jernigan, J.L. Tedesco, R.L. Myers-Ward, C. Eddy Jr., Naval Research Laboratory, X. Weng, J. Robinson, M. Fanton, Penn State University INVITED

In this talk, we present recent progress in epitaxial graphene n-MOSFETs and p-MOSFETs on both SiC and Si substrates for graphene-on-SiC and graphene-on-Si technologies. Both graphene MOSFETs were fabricated in a self-aligned manner on 75 mm wafers and exhibited gate-controlled ambipolar characteristics. For the graphene MOSFETs on SiC substrates, the graphene was grown by Si-sublimation of Si-face 6H-SiC substrates in a commercial Aixtron VP508 epitaxial reactor. For the graphene MOSFETs on Si substrates, the graphene was synthesized by graphitizing a thin 3C-SiC layer grown on float-zone Si (111) substrates using a halogen process. Figure 1 shows sheet resistance maps of 3-inch graphene-on-SiC and graphene-on-Si wafers. Typical Hall mobility ranges from 500 to 2000 cm²/Vs depending on electron carrier density. Both graphene MOSFETs were fabricated with a gate oxide layer and metal gate stack. The gate length was 3 µm. The graphene-on-SiC MOSFETs showed excellent I-V saturation behavior as shown in Figure 2(a). Figure 2(b) shows measured ambipolar behaviors with n-type MOSFET at Vgs = 0 V, while p-type behaviors are observed at Vgs \leq 1.5 V. An I_{on}/I_{off} ratio of 33 was measured. Figure 2(c) shows measured peak transconductance of 600 mS/mm at Vds = 3 V. Figure 3 shows the extrinsic field-effect mobility of 6000 cm²/Vs for electron and of 3200 cm²/Vs for hole obtained at an effective electric field of ~0.27 MV/cm, approaching Dirac point. The measured graphene fieldeffect mobility is eight to 10 times higher than that of ITRS Si n-MOSFETs and ~80 times higher than that of ultra-thin-body SOI n-MOSFETs.

The graphene-on-Si MOSFETs are fabricated in a similar manner. Figure 4 shows measured transfer curves of graphene-on-Si MOSFETs, showing ambipolar behaviors with the Dirac point close to zero gate bias, unlike the graphene-on-SiC MOSFETs. The on-state current is measured at 50 to 125 mA/mm with I_{on}/I_{off} ratio of 3 to 2, respectively. This is the highest performance observed among graphene-on-Si technologies so far. RF performance of graphene FETs will be discussed. This work was supported by DARPA, monitored by Dr. M. Fritze, under SPAWAR contract number N66001-08-C-2048.

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[1] C. Berger et al., Science, vol. 312, p. 1191, 2006; J.S. Moon et al., IEEE EDL., vol 30, p650, 2009

[2] H. Kang et al., ISDRS, 2009

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