Nano-Manufacturing Topical Conference
Room 2018 - Session NM+MS+IPF-MoA

Beyond CMOS: Emerging Materials and Devices

Moderator: C.M. Garner, Intel Corporation

2:00pm **NM+MS+IPF-MoA1 Technology Challenges: The Next 15 Years**, ***P. Gargini***, *C.M. Garner,* Intel Corporation **INVITED**

The semiconductor industry continues to introduce new technologies at the pace dictated by Moore's Law. The International Technology Roadmap for Semiconductors (ITRS) projects that devices can be manufactured with conventional process technology through at least 2020 even though there are significant challenges, but further extensions to extreme CMOS may require new 1D device materials. When extreme CMOS technology has reached the limits of scaling, new devices with potentially new architecture will be needed to provide continued performance improvements. For technologies beyond CMOS, research is proceeding on a number of new alternate "state" devices that would require radical materials with a silicon base. The introduction of new alternate state devices may require the introduction of new interconnect technologies and materials with nm control of properties. The challenges to driving to extreme CMOS and the options for alternate state devices will be discussed. For more information on the International Technology Roadmap for Semiconductors (ITRS): http://public.itrs.net

2:40pm **NM+MS+IPF-MoA3 Beyond CMOS - The Semiconductor Industry's Nanoelectronics Research Initiative**, *H. Coufal,* ***J. Welser,*** Nanoelectronics Research Corporation **INVITED**

The tremendously powerful scaling of transistors, that has enabled Moore's Law for the past forty years, can not continue forever. Some of the reasons, such as the atomistic nature of matter, are obvious. Others are less obvious and will be briefly reviewed before some of the potential alternatives to charge based logic will be analyzed. Such an analysis had the semiconductor industry initiate a Nanoelectronics Research Initiative. The current status of this program will be reviewed.

3:20pm **NM+MS+IPF-MoA5 Nano Manufacturing Challenges**, ***M. Mayberry,*** Intel **INVITED**

Not all "nano" is created equal. Nanostructures formed through tops down construction are widely used in the creation of electronics and have shipped in volume for several years. Nanomaterials that are formed through bottoms-up synthesis or self-assembly are at a comparably early stage in research and development. Combining the two approaches has considerable promise but also significant hurdles to overcome. To illustrate we will discuss three potential applications for nanomaterials and some of the challenges to successful implementation in manufacturing. First consider the problem of forming nanostructures as the size of the features begins to approach molecular dimensions. A 20nm wide structure would only consist of 10 resist molecules side by side if the resist molecule were 2nm in size. That introduces significant granularity which up to now has not been a key concern. This problem could be addressed by designing self-assembly molecules with the proper combination of sensitivity to illumination, chemical properties, and physical size. A second potential application is the formation of dielectrics between metal lines for interconnects. An ideal dielectric is an insulator, strong enough to withstand forces generated with temperature cycling, a barrier to migration of materials, and for performance reasons has a low dielectric constant. These could in principle be met through design of the right building blocks but there are complications with integration in the overall process flow. Finally nanodevices formed through self-assembly (ex. nanotubes) could in principle allow formation of very small devices but the challenge of precision formation, placement, and again integration are daunting. These challenges are not insurmountable but need to be addressed through the right research and development so that the promise of nanomaterials can be achieved.

4:00pm **NM+MS+IPF-MoA7 Metrology for Emerging Devices and Materials**, ***E. Vogel,*** University of Texas at Dallas **INVITED**

Traditional scaling of the CMOS Field-Effect-Transistor (FET) has been the basis of the semiconductor industry for 30 years. The 15 year horizon of the International Technology Roadmap for Semiconductors (ITRS) is reaching a point which +IBw-challenges the most optimistic projections for the continued scaling of CMOS (for example, MOSFET channel lengths of roughly 9 nm).+IB0- As silicon CMOS technology approaches its limits, new device structures and computational paradigms will be required to replace and augment standard CMOS devices for ULSI circuits. These possible emerging technologies span the realm from transistors made from silicon nanowires to devices made from nanoscale molecules. One theme that pervades these seemingly disparate emerging technologies is that the electronic properties of these nanodevices are extremely susceptible to small perturbations in structural and material properties such as dimension, structure, roughness, and defects. The extreme sensitivity of the electronic properties of these devices to their nanoscale physical properties defines a significant need for precise metrology. This talk will provide an overview of emerging devices and materials, and, through example, an overview of the characterization needs for these technologies.

4:40pm **NM+MS+IPF-MoA9 Linking Proteins, Particles and Wires to make Functional Devices: Metrology, Materials and Properties**, ***D.A. Bonnell,*** The University of Pennsylvania **INVITED**

Two issues that are critical, and projected to be limiting, to next generation device technology are metrology at the nanoscale and integration of diverse materials into manufactured devices. The first half of this talk will summarize advances in local measurements of properties and demonstrate new techniques that probe electronic structure and properties in nanostructures and molecular wires. These approaches will be illustrated on 3-terminal configurations that exhibit transistor or memory behavior. Opportunities for exciting advances on the horizon will be presented. The second half of the talk will present strategies for integrating a combination of metal and/or oxide nanoparticles, organic and/or biological molecules on oxide or polymeric substrates in device configurations. The processing approach, Ferroelectric Nano Lithography, induces variations in local electronic structure in substrates to direct assembly of nanostructures with diverse properties into complex patterns, thus overcoming one of the limitations of self assembly. The approach has been used to produce a molecular opto electronic switch.

Plasma Science and Technology
Room 2009 - Session PS1+MS+NM-TuM

Plasma Patterning

Moderator: A. Agarwal, University of Illinois at Urbana-Champaign

8:00am **PS1+MS+NM-TuM1 Resolving Gate Patterning Issues at sub 65 nm Technology Nodes***, **T.J. Kropewnicki**, C.-C. Fu,* Freescale Semiconductor, Inc.

According to the 2005 edition of the International Technology Roadmap for Semiconductors, the physical gate length of high performance transistors at the 65 nm technology node is expected to be 25 nm in 2007, decreasing to 18 nm at the 45 nm node in 2010. Clearly, these goals present a clear challenge to photolithography and etch, which together are responsible for resolving these features on wafers. In addition to the pure scaling aspects of technology progression are the many additional enhancements such as stressors, which are being used to push the performance of silicon circuits. In certain integration schemes, these stressors add complexity to the transistor gate stack and accelerate photoresist bending and line collapse which cause etch masking, and ultimately variable, uncontrollable line widths. This paper will begin with a brief description of the transistor module process flow, highlighting the new challenges introduced to the gate stack etch at sub 65nm technology nodes. Next, a combination of enhancements in the gate photolithography and etch steps used to address these challenges will be presented. Results from these experiments will show a 50% reduction in across wafer line width variation, and a near 100% reduction in the incidence of polysilicon pattern distortion. Finally, the possible mechanisms for the increased levels of polysilicon pattern distortion seen with advanced transistor modules will be discussed.

8:20am **PS1+MS+NM-TuM2 Plasma Impact on ArF Resist Line Edge Roughness***, **J. Thiault**,* LTM / CNRS France, France*; E. Pargon,* LTM / CNRS France*; J. Foucher,* CEA LETI France*; O. Joubert, G. Cunge,* LTM / CNRS France, France

As Critical Dimensions for semiconductor devices shrink too few tens of nanometers, the Line Edge Roughness (LER) or Line Width Roughness (LWR) becomes a critical issue because it can degrade resolution and linewidth accuracy that causes fluctuations of transistors performances. ArF resist patterns present a LWR of about 8 nm after lithography that is possibly transferred into the underlayers during plasma processing steps, resulting in a final LWR above the requirements of the International Technology Roadmap for Semiconductors (ITRS, which tolerates a LWR of around 3 nm for the 65nm technology node). In this study, isolated ArF resist patterns have been exposed to different plasma chemistries under identical processing conditions to investigate the impact of the plasma chemistry on the resist LWR. The sidewall roughness characterization has been performed using 3D Atomic Force Microscope (AFM3D) and top view Scanning Electron Microscope (CD-SEM). Experimental results tend to show that when the plasma/resist interaction is strongly chemically driven, such as in O@sub 2@ or SF@sub 6@ plasmas, with no bias applied to the wafer, the resist sidewalls are not smoothen. However, using plasma conditions where the ion bombardment component of the plasma is increased (by applying a bias power to the wafer), a LWR reduction is measured. This trend has been confirmed by exposing resist patterns to chemically inert plasmas such as Ar plasmas. Moreover, we have investigated plasma curing treatment on resist patterns, currently used in semiconductor manufacturing to reinforce the etching resistance of the resist. In this type of plasma (HBr based) where the ion current density is high and ion energy low, we also observe a decrease in LWR. All these trends suggest that the anisotropic ion flux is responsible for the smoothing of the resist sidewall roughness by eroding the bumps present on the resist sidewall.

8:40am **PS1+MS+NM-TuM3 ArF Resist Friendly Etching Technology***, **T. Hayashi**, Y. Morikawa, K. Suu,* ULVAC Inc., Japan **INVITED**

The requirements for dry etching technology in semiconductor processes beyond 90 nm node come to be very complicated and difficult. In photolithography, the introduction of ArF resist has started. ArF resists generally have very weak plasma resistance and are deformed in the etching process. However, as for the fundamental mechanism of deformation of resists in dry etching, sufficient discussions have not been done yet. So far ArF resist deformation has been thought to be caused by ion impinging damage. However, in our experiments, the deformation was not found in the high density NLD plasma in lower pressure than 1Pa, which gives relatively higher ion flux to the surface. So if ion energy is the main origin of the ArF resist deformation, then the NLD plasma might give a large resist deformation. Contrary to this expectation, however, the etched profiles in the NLD plasma showed low line edge roughness and almost nothing of striation. Considering these facts, the ArF resist deformation is clearly caused by concerted working of ion impinging damage and subsequent radical reactions at the resist-damaged area. This means if either of ion damage or radical reaction is nothing then the ArF resist deformation is nothing or is suppressed considerably lower. Therefore, the lower pressure process below 1 Pa or the lower reactive radical density process is necessitated. The latter is achieved by using highly effective radical scavenger. Generally H or CO has been used as the scavenger of F atoms. However, Br and I may be more effective as the scavenger, because Br and I react with F atoms and form stable inter-halogen compounds. So use of iodine or bromine contained perfluoro-hydrocarbon compounds like CF3I gives the ArF resist friendly etching process. Actually very smooth etched surfaces were obtained for patterned ArF resist/ARC/CAP/low-k/BARC/Si wafers. This work was partly supported by NEDO (New Energy and Industrial Technology Development Organization) in Japan.

9:20am **PS1+MS+NM-TuM5 Plasma Etching of Nano-Scale, Sub-10nm, Features***, **Y. Zhang**, C.T. Black, H.-C. Kim, E.M. Sikorski, T. Dalton,* IBM Research

Features Patterning nano-scale semiconductor features with precision imposes many new challenges for plasma etching. One of the challenges is that as the sizes of nano-scale features shrinking down to the sub-10nm regime, Plasma etching seems to approach to the limits. In this paper, we report the recent results of studying plasma etching of true nano-scale features using tow kinds of nano-sacle patterns. The first type of samples is diblock copolymer (similar to resist) self assembled nano holes and lines. The second kind samples are self-assembled organosilicate (similar to silicon oxide) nano patterns. With samples pattern, arrays of nano holes or nano lines' dimensions in the range of ~10nm, we studied plasma etching challenges for transferring nano-scale patterns into different materials (silicon, and silicon dioxide) in different plasma chemistries and process conditions. By varying the thickness of masks, the characteristics of aspect ratio dependence vs. "real" etching limits due to the sizes of sub-10nm nano-scale features were studied. The impacts of mask selectivity and line edge roughness (LER) to transferring sub-10nm patterns will be also discussed.

9:40am **PS1+MS+NM-TuM6 Nickel Atom and Ion Density in an Inductively Coupled Plasma with an Internal Coil***, **L. Xu**[1]*, University of Houston*; N. Sadeghi,* University Joseph Fourier-Grenoble & CNRS, France*; M.K. Jain, S.C. Vemula, V.M. Donnelly, D.J. Economou, P. Ruchhoeft,* University of Houston

Nanopantography uses monoenergetic ion beams to enable massively parallel patterning of nano-sized features (e.g. 10 nm dia., 100 nm deep holes etched into Si). Deposition of metal nanodots (e.g. Ni) can have applications such as catalysts for the growth of an orderly array of carbon nanotubes. For this purpose, we have developed an inductive plasma source containing a relatively large fraction of Ni@super +@. A two-turn Ni coil immersed in the plasma generates a Ni-containing Ar plasma. Ni was sputtered both from the negatively self-biased coil and from a Ni target powered by a separate rf power. By adding a trace amount of N@sub 2@, gas temperatures T@sub g@ (= rotational temperatures) were derived from N@sub 2@(C-B) spectra. At low powers (capacitively coupled), T@sub g@ derived from the 0-0 band was erroneously high. This was attributed to energy transfer from Ar metastable atoms to the N@sub 2@ C (@upsilon@=0). At high powers (inductively coupled), both the N@sub 2@ 0-0 and 4-4 bands provided the same reasonable T@sub g@ because electron-impact dominates excitation at high power. Optical emission of Ar at 419.8 nm was used to estimate the plasma density, and was in agreement with values predicted from a global model. Ni densities were determined by optical absorption (using a Ni hollow cathode lamp) and were found to increase with pressure and power. The Ni@super +@ densities also increase at higher pressures and powers. Model predictions of Ni@super +@ densities are consistent with metastable Ni@super +@ densities derived from optical absorption. Finally, 50nm dia. Ni islands have been deposited in preliminary nanopantography experiments with the Ni@super +@ beam.

[1] **PSTD Coburn-Winters Student Award Finalist**

10:40am **PS1+MS+NM-TuM9 Bias Frequency Effect on SOC Film Degradation in sub-45 nm Line and Space Pattern SiO@sub 2@ RIE using S-MAP**, ***H. Hayashi***, *K. Kikutani, J. Abe, A. Kojima, T. Oohashi, I. Sakai, T. Ohiwa,* Toshiba Corporation, Japan

Sub-45 nm line and space pattern etching of SiO@sub 2@ film was studied using a stacked mask process (S-MAP) which consists of photoresist, spin-on-glass (SOG) and spun-on-carbon (SOC) film stacked structure. Maintaining pattern integrity becomes more challenging with the decrease of pattern size. Reduction of the hydrogen content of SOC, suppressed the fluorination reaction of its C-H bonds during SiO@sub 2@ etching which lead to line pattern wiggling, and as a result, 56 nm line and space pattern etching was realized.@footnote 1@ This time, the effect of ion energy distribution on SOC degradation in the SiO@sub 2@ etch process was investigated for sub-45 nm line and space pattern etching. The ion energy distribution was varied by dual frequency superimposed (DFS) RIE, using the conditions of 100 MHz rf supply with 3.2 MHz superimposed compared with 100 MHz with 13.56 MHz superimposed. The other SiO@sub 2@ etch conditions were the same, that is, C@sub 4@F@sub 8@ gas chemistry with the same electron density and self-bias voltage (-Vdc) of 6x10@super 10@ cm@super -3@ and 350 V, respectively. As a result, SOC line pattern wiggling was observed in the 3.2 MHz case, but it was suppressed in the 13.56 MHz case, even though the SiO@sub 2@ etch rates were 241 nm/min and 254 nm/min, respectively, and about the same. This shows that, by using DFS RIE with 13.56 MHz superimposed, SOC degradation can be suppressed while maintaining the SiO@sub 2@ etch rate for sub-45 nm line and space pattern etching. The maximum ion energy in the 13.56 MHz case should be lower than that of the 3.2 MHz case under the same -Vdc conditions, because with higher rf frequency, it would have a narrower ion energy distribution. In this way, SOC degradation was suppressed without decrease of the SiO@sub 2@ etch rate. In conclusion, S-MAP combined with 100 MHz/13.56 MHz DFS RIE realized sub-45 nm line and space pattern SiO@sub 2@ etching. @FootnoteText@ @footnote 1@ J. Abe et al., Symp. Dry Process, (2005) 11.

11:00am **PS1+MS+NM-TuM10 High Aspect Ratio (>10:1) Amorphous Carbon Layer Etching Using Soft Etch Capability in a High Frequency Capacitive Coupled Plasma Source Dielectric Etch Chamber**, ***S. Sung***, *J. Wang, S. Ma,* Applied Materials

Amorphous carbon layer (ACL) such as advanced patterning film (APF) is generally selected as one possible hard mask material for variety of dielectric etching application beyond 65 nm technology nodes to improve the etch process margin from reduction of resist thickness. Most of the APF etching application for DRAM, flash and logic technology are done typically on 1 µm film thickness to enable specific integration scheme of nanotechnology. The challenges of etching high aspect ratio ACL features are bowing prevention during etching, hard mask selectivity and the etch rate improvement for throughput concern. In this paper, high aspect ratio (HAR) contact through ACL layer is developed by soft etching capability using high frequency source plasma etch chamber. This development work was done in the dielectric etch chamber consisting of the superimposed dual bias power and a capacitive coupled source power > 100 MHz, which can be operated in either low density process regime for higher resist selectivity, or in high density process regime for profile control, resist integrity, minimal striations and effective chamber cleaning. With high frequency source power, fast etch rate >6000 Å/min of ACL has achieved with minimum hard mask corner chopping from small plasma self bias. All the process trends are characterized with profile control, hard mask selectivity and etch rate.

11:20am **PS1+MS+NM-TuM11 Chamber and Process Development of High Aspect Ratio Deep Trench Si Etch for DRAM Application below 60 nm**, *S. Barth, A. Henke,* Qimonda, Dresden, Germany*; A. Kersch,* Qimonda, Munich, Germany*; M. Reinicke,* University of Technology, Germany*; W. Sabisch,* Qimonda, Munich, Germany*; J. Sobe, A. Steinbach,* ***S. Wege***, Qimonda, Dresden, Germany

For Qimonda's DRAM Technology the deep trench etched into silicon is the base for the capacitor concept. The shrink of lateral dimensions at approximately constant capacity specifications leads to increased deep trench aspect ratio requirements. Therefore high selectivity to the etch mask and excellent uniformity is needed, especially for technologies below 60nm. In this paper we describe the development of a new DT plasma etch chamber and process to fulfill these requirements. Simulations (an equivalence circuit plasma model and surface reaction models) were combined with in-situ plasma measurement techniques (QMS, high resolution OES, IR absorption spectroscopy, SEERS and Langmuir probe sensor wafers) and technological experiments, to characterize hardware features and process conditions. To achieve high Si etch rate and selectivity, plasma density and electron energy distribution in the plasma bulk, and ion energy distribution on the wafer surface can be optimized through multi frequency cathode excitation. The selectivity is further enhanced by using advanced hard mask materials and combining of etching and deposition process regimes. Excellent uniformity has been achieved by new tool components, e.g., multi zone gas distribution and wafer temperature control. In addition, the etch process chamber includes new features for process control, in-situ wafer surface temperature and trench dept measurement. The equipment and process development was accomplished through close cooperation between Qimonda and the tool supplier.

Manufacturing Science and Technology
Room 2018 - Session MS-TuA

Process Integration and Modeling for Nano-scale Semiconductor Devices

Moderator: S. Shankar, Intel

2:00pm **MS-TuA1 Physics of Stress-Induced Performance Gain in Advanced MOSFET Devices***, **M.D. Giles**, S.M. Cea, T. Ghani, R. Kotlyar, P. Matagne, K. Mistry, B. Obradovic, R. Shaheed, L. Shifren, M.A. Stettler, S. Tyagi, X. Wang, C. Weber,* Intel Corporation **INVITED**

Stress-enhanced MOSFET channel mobility has become a key enabler for continued performance improvement in advanced silicon technologies. First introduced at the 90nm node,@footnote 1@ strain engineering is now being widely adopted for 65nm technologies and beyond, and gives a new degree of freedom in delivering improvements in transistor speed and power. Although the piezoresistance effect in silicon has been known for fifty years and biaxial strained silicon investigated for more than a decade, the large mobility gains possible with a dominantly uniaxial strain quickly raised the importance of fundamental understanding of device stress effects, particularly for PMOS. Developing technologies that utilize stress sources similarly requires an understanding of how materials interact to produce a channel stress distribution in the final device. This presentation will review the key physical effects at the process and device levels that contribute to stress-induced performance gain. Through the use of physically-based models of material properties, device fabrication, and device operation, the basis of stress-induced performance gains will be demonstrated and the performance differences between alternative stress configurations explained. @FootnoteText@ @footnote 1@T.Ghani, et al, IEDM Technical Digest, p. 978 (2003).

2:40pm **MS-TuA3 Defect Engineering by Short-Annealing-Time Methods for Ultrashallow Junction Formation***, E.G. Seebauer, **C.T.M. Kwok**, R. Vaidyanathan,* University of Illinois at Urbana-Champaign

Forming extremely shallow pn junctions with very low electrical resistance is becoming a large stumbling block to the continued scaling of microelectronic device performance according to Moore's Law. Manufacturing methods employ rapid thermal annealing after ion-implantation in order to increase the activation of dopants. Empirical results have shown that shorter annealing times and the millisecond time scale by flashlamp or laser methods generally improve dopant diffusion and activation behavior compared with conventional incandescent lamp annealing at 1-2 s time scales. However, an explanation for this effect has been lacking. Via mathematical modeling, we find that increasing the heating rate permits interstitial clusters with dissociation energies lower than the maximum of 3.5-3.7 eV to survive to higher temperatures. This improved survival delays the increase in Si interstitial concentrations near the top of an annealing spike, which decreases the profile spreading. In addition, we present experimental data showing that strong illumination nonthermally influences the diffusion of dopants such as arsenic and boron. Such effects can either enhance or inhibit diffusion depending upon temperature, and depend upon changes in average charge state of both lone interstitials and interstitial clusters. Illumination by incandescent lamps. flashlamps, and lasers employ light fluxes that differ by orders of magnitude, so such nonthermally stimulated diffusion can be used as an additional tool for defect engineering by suitable choice of light source.

3:00pm **MS-TuA4 Virtual Integrated Processing for IC Manufacturing***, R. Chalupa, D.G. Thakurta, L. Jiang, **H. Simka**, S. Shankar,* Intel Corporation

As each new semi-conductor technology becomes more complex, targeted simulations can lead to significant savings in process development time and cost. These are achieved by providing insights into process behavior and quantifying effects of process knobs on performance. Due to the complexity of physical phenomena involved, each process simulator may itself consist of multiple (possibly linked) modules each aimed at different length and/or time scales or different operating regimes. In Electroplating (EP) process for backend (BE) interconnect formation for example, wafer-scale events are often governed by electrostatic potential fields where current distributions are estimated based on local conductivities. Feature scale (less than 1-100 microns) events are often governed by transport-reaction events in shape-changing domains. Availability of accurate simulation tools allows investigations of dependence of a BE step to those preceding it, and its effects on subsequent steps. This "virtual processing" provides information useful in investigation of process input requirements, performance limits, scaling, and other integration issues. One example of process interaction modeling is in EP and CMP areas where models were used to explore film planarity for various realistic chip layouts. Our integrated BE simulator provides an effective way to explore solutions not readily accessible in experiments due to cost and time constraints. These model components have played key roles in developing advanced BE modules, including alternative deposition and planarization processes for 90 nm technology.

3:20pm **MS-TuA5 Semiconductor Materials Challenges and Opportunities for Energy Efficient Power Conversion Technologies***, **M.A. Briere**,* International Rectifier, US **INVITED**

There exists great opportunities to signifcantly impact the world wide energy consumption through the development and implementation of highly efficient power management and conversion technologies. Nearly 25 % of the worlds consumption of oil can be saved by the year 2025 through improvements in electronics used in lighting, transportation, motor control for appliances and power supplies for electronic devices. In order to achieve these results, implementation must be widespread. This requires that the solutions be available without additional system costs. The challenge of providing energy efficiency for free can be met through innovative system architecures and improved semiconductor devices. Significant advances in device and system performance can be achieved through the use of new semiconducting materials. A review of the relationship of device performance and semiconductor material properties for Si, SiC, Diamond and GaN will be presented, as well as a comparison of performance for device structures of diodes, FETs and IGBTs. Material growth techniques such as MBE and MOCVD will be compared for these purposes. A summary of the state of the art in the material properties and device characteristics for these alternatives to the present Si offerings will be made. Critera for large scale manufacturing using these materials and growth techniques will be presented.

4:00pm **MS-TuA7 Electrochemical Planarization of Copper Surfaces with Sub-Micron Features***, **R. Chalupa**, A.N. Andryushchenko, J. Han, T. Ghosh, S. Shankar, P. Fischer,* Intel Corporation

Electrochemical planarization (ECP) of copper surfaces in a phosphoric acid-based electrolyte solution is discussed. A first-principles, quantum-chemistry modeling work is presented that further validates the water-facilitated (and water rate limited) chemistry model for copper oxidation at the anode. This model has been previously deduced by other researchers@footnote 1,2,3@ based on electrochemical experiments. Resulting water-limited model is validated against experimental data and applied to study the planarization behavior of a set of surface features. Aspect ratios and dimensions of these features were chosen to represent realistic (non-idealized, low aspect ratio structures) post Damascene electroplate surface topography. Results are presented in a form of remaining feature amplitude versus mean copper thickness removed@footnote 4@ - allowing at-a-glance evaluation of the process against desired targets. The dominant effects of the mass transport boundary layer (BL) thickness on this planarization efficiency are discussed as are the challenges seen at typical flow conditions in ECP systems. Impact of changing the BL thickness and the requisite modulation of flow conditions analysis is included. Insights into practical challenges associated with BL build-up transient and associated surface roughening are summarized@footnote 5@. Challenges of applying ECP as a straightforward substitute to the robust CMP process are significant. Practical modifications to upstream process flow to enable ECP would include optimized electroplating process or a CMP pre-processing step. @FootnoteText@ @footnote 1@R. Vidal, A. C. West, J. Electrochem. Soc., 142, 2682 (1995). @footnote 2@R. Vidal, A. C. West, J. Electrochem. Soc., 142, 2689 (1995). @footnote 3@B. Du, I.I.Suni, J. Appl. Electrochem., 34, 1215 (2004). @footnote 4@A. C. West, I. Shao, H. Deligianni, J. Electrochem. Soc., 152, C652 (2005). @footnote 5@D. Padhi, J. Yahalom, S. Gandikota, G. Dixit, J. Electrochem. Soc., 150, G10 (2003).

4:20pm **MS-TuA8 Large-Scaled Line Plasma Production by Evanescent Microwave in a Narrow Rectangular Waveguide***, **E. Abdel Fattah**, S. Fijii,* ADTEC Plasma Technology Co. LTD, Japan*; H. Shindo,* Tokai University, Japan

Long line-shaped plasmas are attractive for use in material processing in manufacturing industries, such as .at panel displays (FPDs) and surface modification of large- area thin films. Several types of plasmas have been developed to meet those needs. In this study, long line-shaped microwave plasma was generated employing a narrow rectangular waveguide. The wavelength of a microwave in a waveguide increases in accordance with

the width of the waveguide. The objective of this work is to provide a method of large-scaled line plasma production by employing narrow width rectangular waveguide. A narrow and flattened rectangular waveguide was prepared with the internal dimensions of 1000mm length, 59 to 62mm width and 5mm height. The waveguide was connected to a TE10 mode rectangular waveguide (WST-AD standard). In this narrowed waveguide, the microwave is cutoff, but the evanescent wave is employed to produce the plasma. Two types of line-shaped plasmas was generated; one being a cavity type and the other a slit type. The cavity type line-shaped plasma has a quartz tube in the waveguide as a discharge tube and helium gas as well as argon was supplied into the quartz tube through orifices of the waveguide. The slit type line-shaped plasma has a slit on its side. A quartz tube as a discharge tube was set beside the slit and helium gas as well as argon gas is supplied into it. Electric field intensity and optical emission intensity were then measured. Uniformity of line-shaped plasmas was improved by reducing the width of the waveguide and the microwave power in both types of line-shaped plasmas. In particular, the uniform line plasma could be produced as long as 1000mm in length at 100 Torr pressure. The uniformity was confirmed by both the measurements of electric field and optical emission intensity.

4:40pm **MS-TuA9 Innovative Studies for Ultra High Aspect Ratio Deep Trench Etch*, S. Pamarthy*, *F. Ameri, D. Gutierrez, D. Scanlan, F. Schaeftlein,* Applied Materials

A key challenge that DRAM manufacturers are facing today is achieving very high aspect ratios in deep trench etch. Future DRAM technology shrinks require development of hardware and process solutions to etch deep trench features at aspect ratios >80:1, for which there is no known available solution today. This paper describes how this key technical challenge can be overcome to implement a manufacturing solution to meet the aspect ratio requirements for DRAM DT technology needs of 65nm and beyond. The entire development path is traced, from initial plasma generation and gas flow modeling studies, early concept experiments involving plasma characterization, and process condition explorations and eventually to a final reactor design, including the innovation of multiple uniformity tuning knobs. The paper also focuses on studies done with each of the following hardware/process tests: Gas Flow Ratio Control (FRC), Dual Zone Coolant Ceramic ESC and Independent Gas Injection (IGI) independently and the impact these tests have on some critical aspects of deep trench etch such as center to edge trench depth non-uniformity, center to edge bottom CD uniformity, mask selectivity, Top CD widening, and mask remaining uniformity across the wafer. The study shows that some of the limitations of the current production chambers can be improved with these potential features. The paper also talks about how a future reactor can potentially be the only chamber of its kind with a clear capability to tune the capacitance of each DRAM cell across the wafer using these innovative features. For selectivity improvements, studies with new silicon source gases such as SiF_4 and $SiCl_4$ as additional sources for re-deposition during the etch process are discussed.

Manufacturing Science and Technology
Room 2018 - Session MS-ThA

Sensors, Metrology, and Control

Moderator: A.C. Diebold, SEMATECH

2:00pm **MS-ThA1 Three-dimensional Imaging of Nano-Voids in Copper Interconnects using Incoherent Bright Field Tomography**, *P. Ercius, M. Weyland,* Cornell University; ***D.A. Muller,*** Cornell University, US; *L.M. Gignac,* Thomas J. Watson Research Center **INVITED**

As integrated circuits have shrunk, conventional electron microscopies have proven inadequate for imaging complicated interconnect structures due to the overlap of features in projection. These techniques produce transmission functions with a non-monotonic dependence of intensity on thickness for common microelectronic materials, making them unsuitable for tomography. We report the use of an incoherent bright field imaging technique in a scanning transmission electron microscope optimized for the three-dimensional reconstruction of thick copper microelectronic structures. Predictable behavior of the signal in samples up to ~1 micron thick allows us to reconstruct and quantify the shape and volume of stress voids within Ta-lined interconnects as well as analyze the liner roughness in 3 dimensions.

2:40pm **MS-ThA3 Critical Dimension Metrology: A Comprehensive Evaluation of Current Techniques in Spectroscopy-Based Scatterometry**, ***C. Saravanan***, *Z. Liu,* Nanometrics Inc

In recent years scatterometry has evolved into a reliable, non-invasive and fast technique to characterize critical dimensions (CD) in semiconductor device fabrication. Both polarized-light Normal Incidence Spectroscopy (NIS) and Spectroscopic Ellipsometry (SE) have been successfully used as competing techniques in CD metrology. While several studies have been performed to evaluate these techniques, a thorough evaluation of the 'optimal space' of applicability for these individual techniques does not exist. Furthermore, very little is known about the combined NIS and SE approach as an alternate method for CD metrology. In this paper we first explore 'regions' of optimal applicability of these three techniques (NIS, SE and NIS+SE) by performing simulations on multiple structures with varying heights, sidewall angles, optical properties and pitch (360nm, 180nm, 90nm, 45nm, 32nm and 16nm). We show that regions of optimal applicability exist for all three techniques. We also perform experimental studies for some typical applications and demonstrate the benefit of using combined analysis of NIS and SE to limit parameter correlation and to enhance sensitivity. This is particularly important for scatterometry applications in future technology nodes with much smaller device dimensions.

3:00pm **MS-ThA4 Low Coherence Optical Interefferometry and Raman Scattering Spectroscopy for Stress Tensor Measurements**, ***W.J. Walecki,*** *T. Azfar, A. Pravdivtsev, A. Koo, J. Ryu,* Frontier Semiconductor

In this paper we discuss accuracy and reproducibility of two techniques for metrology of stress tensor in semiconductor wafers: novel combined IR low coherence optical interefermetry@footnote 1@ allowing simultaneous measurement of wafer topography and wafers and thin film thicknesses, enabling calculation of all in plane stress tensor components, and high precision tensor resolved Micro-Raman spectroscopy. Typical micro-Raman measurements are performed in backscattered geometry. Observed stress dependent Stokes shift is related to stress in the material using specific stress tensor model typically derived on a basis of symmetry considerations,@footnote 1,2@ the usual reported reproducibility of the stress measurement of the order of 10 MPa-30 MPa,@footnote 2,3@ which corresponds to reproducibility of the Stokes shift of the order of 0.05 cm-1). By applying very large focal length grating spectrometer (effective focal length 1.34 m), and proprietary thermal drift compensation we were able to achieve thermal stability of the better than 0.0002 cm-1 / min which allows us to further improve reproducibility. We also propose two methods for recovering three and six stress tensor components in cubic crystals (such as Si/SiGe) on microscopic scale. @FootnoteText@ @footnote 1@ W.J.Walecki, A. Pravdivtsev, K. Lai, M. Santos, G. Mikhaylov, A. Koo, in ''Characterization and Metrology for ULSI Technology 2005'', edited by D.G. Seiler, et al, American Institute of Physics, p. 338- 342, 2005@footnote 2@ V. T. Srikar, A. K. Swan, M. S. Unlu, B. B. Goldberg, and S. M. Spearing, IEEE Journal of Microelectromechanical systems, Vol. 12, No. 6, December 2003, pp. 779-787@footnote 3@ Ingrid De Wolf, Chen Jian, W.Merlijn van Spengen, Optics and Lasers in Engineering 36 (2) (2001) pp. 213-223.

3:20pm **MS-ThA5 Micro-Probe CV and IV Analysis of Thin Dielectric Films in Product Wafer Scribe-Line Structures**, ***V.V. Souchkov,*** *T.M.H. Wong, V.N. Faifer, M.I. Current,* Frontier Semiconductor

A 50 µm metal probe has been coupled with pattern recognition optics and a precision stage for automated CV and IV testing of dielectric layers in scribe-line test structures on IC product wafers. Highly repeatable contact conditions are obtained though the use of a MEMS-based torsion balance spring mounting which provides capacitance measurements within 0.1% for repeated landings of the probe. High repeatability capacitance measurements provide for correspondingly high quality determination of dielectric characteristics, EOT, Vfb, Dit, Na and Qeff, from CV analysis. Dielectric leakage and breakdown characteristics, including Vbd, Qbd and TTBD, can be obtained for positive and negative ramped bias conditions. Examples of dielectrics include thin (1 nm) SiO@sub 2@, oxy-nitrides and Hf-based oxides as bare films and incorporated in capacitor structures.

3:40pm **MS-ThA6 Characterizing Copper Lines for Advanced Interconnect Using Normal Incidence Scatterometry**, ***Z. Liu,*** *Y. Hao,* Nanometrics Inc.

With the continuous evolution of smaller device dimensions and denser circuit integration, copper interconnect with low-k dielectrics have been the most popular solution for future technology generations. In copper interconnect, one of the major challenges is the dimensional control of the interconnect features, which is critical to achieve necessary circuit performance of the device. To achieve best device performance, there is limited tolerance of the profile variation in interconnect structures. This dimensional control requirement demands metrology solutions to characterize the interconnect structures in all metal levels. In this paper we propose to use normal incidence scatterometry to characterize the copper lines (line width and height) at various metal levels. Normal incidence scatterometry uses a polarized broadband light source to measure the reflectance spectrum of the grating line structure. Using the modeling technique, profile information including line width and height can be determined. In this work we measure copper grating line structures at different metal levels (M1, M3 and M7) after each chemical mechanical polishing. These structures correspond to different copper line-widths ranging from 0.09 to 0.8 um. Structures with copper lines either parallel or perpendicular to each other between adjacent metal levels are studied. Advanced modeling techniques are used to decouple spectral contributions between the top metal level and the metal levels below. The measurement results are compared with results from other reference techniques, e.g. X-SEM and a very good agreement is demonstrated.

4:00pm **MS-ThA7 Leakage Current and Dopant Activation in Ultra-Shallow Junctions Following Ms-Anneals Measured by Non-Contact Junction Photo-Voltage Methods**, ***V.N. Faifer,*** *T.M.H. Wong, M.I. Current,* Frontier Semiconductor

Leakage current and dopant activation characteristics of ultra-shallow junctions formed with ms-timescale anneals, which provide the beneficial result of minimal dopant diffusion, are highly sensitive to damage accumulation effects during the implantation of dopants, pre-amorphizing and various cocktail (C, F, S, etc.) ions. Damage accumulation levels are a result of the choice of ion, energy, dose and target material as well as process conditions such as beam current density, wafer temperature and beam scanning details for each implant cycle. The residual damage levels after annealing depend on the depth and character of the accumulated damage and the time-at-temperature ramp and ambient atmosphere conditions during each annealing step. For ms-timescale anneals which involve the use of scanned and pulsed energy deposition, the uniformity of the dopant activation and damage annealing process is strongly dependent on the spatial extent and overlap strategies used for the energy deposition beam used for heating. Measurement of junction characteristics through analysis of surface photo-voltage levels provides non-contact, high precision and independent measures of sheet resistance and leakage current density over 4 orders of magnitude. Discussion of leakage current effects will include the impact of background doping and defect density on carrier recombination and trap-assisted tunneling mechanisms. High-resolution (1,000 points per wafer) mapping of sheet resistance and leakage current variations provides rapid feedback for process evaluation of implant and annealing process equipment and correlation of conditions which result in favorable dopant activation and damage annealing.

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