Plasma Science and Technology
Room 3rd Floor Lobby - Session PS2-TuP
Etching and Process Integration Poster Session

PS2-TuP1 Development of a Dry Etching Profile Simulator in a High-Density, Low-Pressure Plasma, ***J. Saussac***, *A. Quintal-Leonard, J. Margot,* Université de Montréal, Canada; *M. Chaker,* INRS-Energie, Matériaux et Télécommunications, Canada

The development of new sub-micron technologies requires a fundamental understanding of device fabrication processes in order to be able to push the technology to its limits. In this context, numerical simulations are of great interest for providing insights into the physics underlying various processes and therefore helpful for optimizing the experimental conditions. Our ultimate purpose is to develop a 2-dimensional plasma etching simulator devoted to the determination of the etch profile evolution of complex oxides in a high-density reactive plasma. Our approach consists in a two dimensional cellular discretization of the plasma, mask and material domains; each cell is initially set to the same size and includes the same number of atoms. Ion transport from the plasma to the surface is simulated by a Monte Carlo technique. Testing of the model is performed by comparing its predictions to existing experimental measurements of silicon sputter-etched patterns. As only pure physical etching is considered, the atomic population of each cell evolves according to the etch yield, the cell passing from an unetched to an etched state when the number of atoms by cell falls below a threshold. Once the model validated for silicon sputter-etching, it is planned in a second step to introduce in the model the chemical aspects required to investigate the etching of complex oxides like SrTiO@sub 3@ in a halogenated plasma.

PS2-TuP3 A Comparative Study of Wafer Edge, Backside and Bevel Etching Properties for Oxide, TiN and Amorphous Carbon Films with Torus-Shaped Capacitive Coupled Plasma Source, *S.-H. Cho,* ***J.-H. Yang***, *I.-S. Choi, J.-K. Kim, H.-J. Lee, B.-H. Choi, J.W. Kim,* HYNIX Semiconductor Inc, Republic of Korea

The film residues polymer that are generated during the semiconductor device processing on the wafer edge, backside and bevel area are known to be severe particle source. These areas need to be cleaned to prevent the particle from inflowing into the pattern area. In this study, the bevel etching properties for oxide, TiN and amorphous carbon film with torus-shaped capacitive coupled plasma source are examined to find ways to remove harmful film residues polymer on the wafer edge, backside and bevel area. The optimum plasma process conditions without plasma damage on wafer pattern area will be discussed as a function of processing parameter such as pressure, power and gas ratio.

PS2-TuP5 Etching of Ultra-low-k BEOL Material with High Density Plasma, ***T. Nishizuka***, *T. Nozawa,* Tokyo Electron, LTD., Japan

As the design rule of device is evolved, k value of BEOL dielectric material is required to be lower, and its mechanical strength and plasma resistance become also lower. For the current generation whose k is 2.7~3.0, plasma condition of dielectric etching can be still similar to SiO2 etching condition with low plasma density and high ion energy. For the future generation whose k is less than 2.5, however, different plasma condition with high density and low energy is supposed to be applicable since the material become like organic and porous. In this study, we examined RLSA (Radial Line Slot Antenna) microwave plasma to low-k etching, and found extremely low ion energy (RF bias Vpp<250v) resulted in smooth resist mask surface and via sidewall keeping enough etch rate. Furthermore it appeared that the selection of bias power frequency was effective to RIE lag control.

PS2-TuP6 Study on the Plasma Damage by Spacer Oxide Etching of MOSFET Device, ***H. Ahn***, *J.S. Lee, S.B. Kim, K.D. Kim, B.H. Lim, D.G. Choi, D.S. Kim, Y.W. Song, J.W. Kim,* HYNIX Semiconductor Inc., Republic of Korea

Plasma etching is widely-used tool for the manufacturing of large scale integrated electronic device. In dry etching process, the plasma damage is able to cause dielectric breakdown or severe change of electrical properties, such as threshold voltage, breakdown voltage, and so on. Recently, the researches on these areas have been widely studied, it is well known that uniform plasma is the best solution to minimize charging effect. In this paper, the impact of plasma damage on the MOSFET during spacer oxide etching that is necessary for the formation of LDD structure MOS transistor after deposition of sidewall dielectric layer is studied. Especially, this work focused on the damage effect of on-off transient from the viewpoint of device parameter. Physical properties are characterized by Secondary Ion Mass Spectroscopy (SIMS), Transmission Electron Microscopy (TEM), Auger Electron Spectroscopy (AES) and so on. It is found that on-off transient damage is one of the most important factor to affect the PMOS device characteristics.

PS2-TuP7 Plasma Chemistries for High-Aspect-Ratio Dielectric Etching Beyond 65 nm Node, ***T.L. Anglinmatumona***, San Jose State University; *C.T. Gabriel,* Advanced Micro Devices

The transition from saturated (c-C4F8, C-C) to unsaturated (1,3-C4F6, C=C) plasma gases was found to lessen the challenges of low selectivity and ARDE. The shrinking diameter of the via-hole due to scaling feature sizes is inducing an austere list of etch challenges. Saturated chemistries are known to generate large molecular-weight radicals that lead to poor etch performance with increasing aspect ratios. Due to the changing dynamics of device sizing, saturated chemistries offer limited etch performance which is mainly driven by their high energy thresholds and bond decomposition scheme. Data in this research show the chemistry of hexafluorobutadiene (1,3-C4F6) is helping to enable good etch performance with increasing aspect ratios beyond 65 nm. The etch selectivity was improved by 2X. ARDE was reduced and showed a via-depth improvement of 11.5%.

PS2-TuP8 Formation of Silicon Nitride Nano-Pillar Hard-Mask Patterns in Dual-Frequency Superimposed Capacitively Coupled Plasma and Their Application to Nano-Scale Si Etching, ***C.K. Park***, *C.H. Lee, H.T. Kim,* Sungkyunkwan University, Korea; *N.-E. Lee,* Sungkyunkwan University, korea

Fabrication of silicon nano-scale structures has attracted much interest because of distinctive differences in the etch properties of these nano-scale hole compared with large-size diameter hole (@>=@ 100 nm). However, it is difficult for conventional optical lithography techniques to make patterns smaller than a light wavelength. Nano-scale etching using nano-pillars formed by non-lithographic method can be very useful for under standing the etch characteristic of nano-scale patterns. In this work, we investigated nano-scale etching of silicon pattern with the diameter less than 30-nm using the silicon nitride nano-pillars as hard-mask or lift-off mask. Silicon nitride layers were etched with CH@sub 2@F@sub 2@/H@sub 2@/Ar dual frequency superimposed capacitively coupled plasma (DFS-CCP). During the etching process the CF@sub x@ polymer nano-dots are formed on silicon nitride surface, which leads to the formation of silicon nitride nano-pillars. Nano-scale Si pillar etching using the silicon nitride nano-pillar hard-mask or Si hole pattern etching using polymer mask generated by lift-off method were carried out. Etching characteristics of nano-scale silicon patterns will be discussed in detail in conjunction with the silicon nitride nano-pillar hard-mask fabrication.

PS2-TuP9 Development of Dual-Frequency Inductively Coupled Plasma and Control of Plasma Parameters Changing the Power Ratio between High- and Low-Frequency rf Sources, ***S.-H. Seo***, Korea Advanced Institute of Science and Technology, Republic of Korea; *H.-S. Lee,* Korea Advanced Institute of Science and Technology, South Korea; *H.-Y. Chang,* Korea Advanced Institute of Science and Technology

A novel dual-frequency inductively coupled plasma source which was developed for high-density plasma CVD process was presented. Two coaxial planar-type antennae consisting an outer single-turn antenna with a diameter of 300 mm and an inner multi-turn antenna were used for the plasma generation and applied by two rf powers with different frequency. The two rf power sources with the frequencies of 2 and 13.56 MHz respectively were used in the experiment. A Langmuir probe with four chock filters for the rf compensation for the primary and the second harmonic rf noises of each frequency was used to characterize the dual-frequency inductive plasma. It was found that the electron temperature can be controlled by changing the power ratio between two rf sources and is ranged within the electron temperatures achieved in the single-frequency inductively coupled plasma with each frequency. Also, the power ratio between two frequencies and the configuration of two antennae was found to control the plasma uniformity in the radial direction. Here, the experimental results such as the diagnostic and CVD process results will be presented and the effect of two rf powers on the plasma characteristics and the CVD process will be discussed.

PS2-TuP10 Silicon Surface Treatment of Contact Hole in Memory Device by Downstream Plasma, ***C.W. Kim***, PSK-inc, Korea, Korea, Republic of; *C.W. Lee, H.B. Seo, K.T. Kim, J.K. Yang,* PSK-inc, Korea

Silicon surface of contact hole has been treated by fluorine based plasma using downstream type ICP source. Silicon etch rate and uniformity had been investigated on 12 inch blanket wafer as a function of process parameters. The profile of etch rate map is changed from center high to edge high etch rate tendency by controlling total gas flow rate and this make it possible to control etch uniformity. The etch selectivity of silicon to silicon nitride, as SAC barrier material, is studied with the various gas mixture ratio of feed stock gas. Commonly higher etch selectivity is obtained under the high silicon etch rate condition due to the difference of etch characteristics between silicon and silicon nitride film but higher selectivity more than 7:1, silicon to nitride, can be achieved over wide range of silicon etch rate by adjusting gas mixture ratio. Finally, the etch uniformity and etch profile of bit line contact and storage node contact hole is examined by TEM on 12 inch whole pattern wafer.

PS2-TuP11 The Behavior of Polymer Film Deposition during Etching the Oval Contact Holes, ***S.-I. Cho***, Samsung Electronics Co. LTD, South Korea; *S. Lim,* Samsung Electronics Co. LTD, Korea; *H. Baik,* Samsung Advanced Institute of Technology, Korea; *Y. Lee, C.-J. Kang, H. Cho, J.-T. Moon,* Samsung Electronics Co. LTD, Korea

Recently, the distorted pattern transfer during the high aspect ratio contact etching process has been reported. The reason of the deformation seems to be the result of non-uniform polymer deposition and/or the deflection of ion trajectory. This study is intended to clarify the behavior of the polymer deposition and its effect on the pattern deformation. The thickness of the polymer films on the sidewall of oval holes after etching was measured by cross-sectional TEM and SEM. The samples with carbonic masking layer were prepared after etching with C4F6, Ar, and O2 chemistry. The aspect ratio of the holes was 15. The thickness of the deposited film is variable with respect to the shape and the position of the holes. A thicker film is deposited along the sidewall of the shorter axis of the oval pattern than the sidewall of the longer axis at the middle of the holes. However, a thinner film is deposited along the sidewall of the shorter axis at the opening of the holes. This difference of film thickness can be explained by the behavior of sputtered masking materials and the randomly moved polymer radicals. The differently deposited films on the sidewall of the holes result in the deformation of the transferred pattern. Different film thickness at the opening produces the asymmetric local electrical field. The electric field results in bending the ion trajectory to the longer axis. Because of the ion accumulation, the profile in the longer open axis becomes more vertical. Moreover, the thicker film on the sidewall of shorter axis at the middle of the holes prevents from etching the sidewall. Therefore, transferred patterns in the bottom of the holes become more oval shaped than patterns in the masking layer.

PS2-TuP12 Empiric Study on the Effects of Two Different Film Stack Approaches on Gate Etching in Typical High-Density Plasma for Advanced Embedded Logic & Flash Systems, ***S. Sciarrillo***, STMicroelectronics, Italy

Advanced Embedded logic & flash memory systems (120nm and below) requires necessarily new and complex solutions in terms of process integration. An empiric study on the effects of two different film stack approaches on gate etching in typical high-density plasmas will be discussed in this paper. Profile evolution of a high aspect ratio dense pattern could change in significant way if between photoresist (193nm) and polysilicon a thin oxide layer has (or not) been grown by a previous oxidation. In the top-poly oxidation approach, for the first time, evident notching at the middle height of the structure (not at the bottom as typically known) has been seen; the observed phenomenon depends on the pattern density and the electrical connection status of the polysilicon lines. An extensive morphological analysis has been performed and the results suggest the presence of three correlated effects during the etching: a) electron shading; b) resist bending (depending on the local charging of the neighboring surfaces); c) notching mechanism.@footnote 1@ Dependence on the aspect ratio (different resist thickness) and on the film stack (w/wo top oxidation) has been empirically characterized. A Process window on the different etching steps has permitted to identify the strategy to reduce substantially the morphological issues, e.g. towards a straight gate profile. Achieved results are consistent with the electron shading effect, notching theory and with the relationship between the resist thermo-physical properties (T@sub g@) and its thickness.@footnote 2@ @FootnoteText@ @footnote 1@ R.J. Dhul, S.J. Pearton (Eds.), Handbbok of Advanced Plasma Processing Techniques, Springer Ed., 257-308 (2000)@footnote 2@ N. Vourdas, A.G. Boudouvis, E. Gogolides, Microelectronic Engineering 78-79, 474 (2005)

PS2-TuP13 A Comprehensive Characterization of the Silicon Substrate Surfaces Damaged by Plasma Processes and the Impacts on Future Scaled Devices, ***K. Eriguchi***, *K. Nakamura, M. Kamei, D. Hamada, H. Fukumoto, K. Ono,* Kyoto University, Japan

The surfaces of silicon substrates after the plasma exposure have been investigated by primarily using optical techniques; photoreflectance (PR) spectroscopy and spectroscopic ellipsometry. Electron Cyclotron Resonance (ECR) and DC plasma sources with Ar-based gas mixtures were employed to induce the defect generation in the substrates for various biasing conditions, i.e., ion bombardment energies, and process durations. The PR studies with an s-polarized probe beam at the 80° grazing-incidence angle have revealed the decrease in the reflectance change by the plasma exposure, but no significant shift of the optical transition energy at around 3.3-3.4 eV, indicating that the carrier recombination centers are generated in the vicinity of the interface between the natural oxide layer and silicon substrate. The ellipsometric analysis based on the classical dispersion has identified the damaged-layer and determined the thickness as thinner than 6 nm for all the process conditions conducted in this study. The substrate resistivity measurement has shown the increase in the standard deviation of the values by the plasma exposure. The defects in the substrate surface region were further identified distinctly by the present PR setup for the sample treated by the ECR plasma system under no biasing condition (Ar/O@sub 2@ gas mixture). Based on this new finding, we conclude that the thickness and electrical property of the plasma-damaged layer should be taken into account for future scaled devices, e.g., those with the junction depth shallower than 10 nm.

PS2-TuP15 Deposition and Characterization of SiO@sub x@N@sub y@Bottom Anti Reflective Coating (BARC), ***X. Peng***, *Z.Y. Wang, D. Dimtrov, S. Xue,* Seagate Technology

With the shrinking of the critical feature line width in both semiconductor and storage industries to meet the ever-increasing requirement for high package density/recording density, the control of the critical feature dimension at sub 100 nm is a big challenge. The industry trend is using shorter wavelength (193 nm for example) lithography for better resolution and using BARC for minimizing standing wave formation and better CD control. Matching the optical constants (n, k) between the BARC, photo resist and underlayer is critical in eliminating the standing waves. SiO@sub x@N@sub y@ and SiO@sub x@C@sub y@ are two attractive inorganic BARC candidates, due to their adjustable optical constant by varying the deposition parameters and their etching compatibility with standard plasma process. SiO@sub x@N@sub y@ films have been prepared by Plasma Enhanced Chemical Vapor Deposition (PECVD) approach at various process parameters, such as SiH4 flow rate, SiH@sub 4@/N@sub 2@O ratio and NH3 flow rate. SiO@sub x@N@sub y@ films have been characterized using x-ray photoelectron spectroscopy (XPS) for chemical composition depth profile, FTIR for local chemical bonding and ellisometry for optical constants. It has been demonstrated that the refractive index of SiO@sub x@N@sub y@ can be tuned from 1.6 to 2, while k can be adjusted from 0.1 to 0.9. Inductively coupled plasma (ICP) has been used to etch the SiO@sub x@N@sub y@ film for pattern transferring capability study with CHF@sub 3@+O@sub 2@ chemistry. CN emission line at 387 nm wavelength was used for endpoint. The profile of the etched SiO@sub x@N@sub y@ is studied by cross-section transmission electron microscopy (TEM). Finally, the SiO@sub x@N@sub y@ BARC application in combination with hard mask has been discussed

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