Tuesday Afternoon, November 14, 2006

Plasma Science and Technology
Room 2011 - Session PS2-TuA

Etch for Advanced Interconnect II

Moderator: G.S. Oehrlein, University of Maryland

2:00pm **PS2-TuA1 Highly-Selective and Low-Damage, Damascene Processes in Robust Porous Low-k/ Cu Interconnects***, **H. Ohtake**,* Tohoku University, Japan **INVITED**

To reduce the cross-talk and power consumption among the on-chip interconnects, low-dielectric constant (low-k) films have been introduced. However, there are several problems on etching/ ashing process, such as the low etching selectivity to the mask, and the ashing damage of low-k film. In this paper, we will show 2 types of highly-selective and low-damage processes, (I) multi-hard-mask process and (II) advanced neutral beam process. We developed the 4 layered multi-hard-mask process without ashing damage. By controlling the radical ratio of carbon to oxygen, the etching selectivity to SiO@sub 2@ hard mask is kept high. The parasitic capacitance of Cu/ porous SiOCH in this process reduced about 7 % as compared with that in conventional via first DD process because of ashing-free process. The hard mask process is effective to reduce the damage, however, it is difficult to control the etching uniformity and hard-mask shouldering for various damascene structure. As an advanced process, we developed a newly advanced neutral beam system. The etching selectivity was drastically improved, and ashing damages were reduced significantly. We speculated that this is due to the elimination of exposure of ultraviolet light. Accordingly, the neutral beam system is a promising candidate for use in porous low-k damascene processes beyond 45nm node ULSIs.

2:40pm **PS2-TuA3 Plasma Confinement in Multi-frequency Plasma Process Chamber***, **K. Bera**, D.J. Hoffman, M. Kutney,* Applied Materials, Inc.

A production-worthy plasma process chamber needs to confine plasma to minimize chamber contamination, to reduce cleaning time and cost, and to minimize process drift. The process chamber needs to achieve high flow rate at low pressure for critical etch applications. One method to confine plasma can be the use of slotted confinement ring. However, a slotted confinement ring generates significant pressure gradient that prohibits low pressure high flow operation. In addition, ignition of plasma in the peripheral region can lead to process drift that is detrimental to process performance. An annular confinement ring design confines plasma for both VHF and HF operating conditions. The annular ring design is optimized using plasma and flow simulations to ensure plasma confinement and enhance flow conductance. Higher flow conductance leads to lower pressure on the wafer enhancing operating window that allows us to achieve desired process characteristics for critical etch processes. The annular confinement ring avoids parasitic plasma improving productivity. To further enhance plasma confinement, an innovative concept of impedance confinement has been analyzed using plasma simulation. An impedance parameter has been defined, and optimized so as to achieve highly confined plasma. The optimized design of confinement ring with impedance confinement is implemented and verified experimentally for both VHF and HF operating conditions. Annular confinement ring design with impedance confinement not only confines plasma to minimize chamber contamination, reduce cleaning time and cost, but also avoids parasitic plasma to improve productivity, and increases flow conductance to enhance operational window.

3:00pm **PS2-TuA4 Scaling of Dual Frequency Capacitively Coupled Plasma Etching Tools Above 100 MHz****, **Y. Yang**, M.J. Kushner,* Iowa State University

Capacitively coupled dual frequency reactive ion etching reactors allow, in principle, independent control of the ion flux and ion bombardment energy which is important for obtaining high selectivity. There is great interest in extending the high frequency to values approaching or exceeding 100 MHz to increase the proportion of power dissipated in electron heating while lowering the electron temperature. These trends are believed to produce more favorable dissociation pathways in, for example, fluorocarbon etching. In this talk, results will be discussed from a computational investigation of dual frequency RIE reactors for high frequencies exceeding 100 MHz. This study was performed with a two-dimensional hybrid-fluid model. To properly address the coupling between the electric field and electron transport under high frequency conditions, a fully implicit electron transport algorithm was developed. Spatially dependent electron energy distributions generated by a Monte Carlo simulation, which properly captures the high frequency heating, provide excitation rates. Results from studies in rare gases and fluorocarbon gas mixtures (e.g., Ar/C@sub 4@F@sub 8@/O@sub 2@) will be presented as a function of the high frequency while keeping power constant. Assessments of the change in dissociation pathways, radical fluxes; and ion energy and angular distributions to the substrate will be presented. @FootnoteText@ *Work supported by the Semiconductor Research Corp. and the National Science Foundation.

3:20pm **PS2-TuA5 Patterning of Narrow SiOCH Trenches using the Late Porogen Removal Process***, **T. Chevolleau**,* LTM-CNRS-France, France*; D. Eon,* CNRS-LTM-France*; M. Darnon,* CNRS-LTM-France, France*; T. David,* CEA-LETI-France, France*; L. Vallier,* CNRS-LTM-France*; O. Joubert,* CNRS-LTM-France, France

In CMOS technology, the dominant strategy to achieve future generation of ultra low-k interlayer dielectric materials with a dielectric constant close to 2.2 is to introduce porosity into a SiOCH matrix. However, porous materials are very sensitive to ash and etch plasma exposures and one of the integration challenges is to reduce the impact of these plasma processes on the low-k modification. To solve this issue, one of the emerging solutions is the late porogen removal process. In this approach, the porosity in SiOCH is generated by a sacrificial porogen (carbon based polymer) which is desorbed after patterning or copper filling. These hybrid materials are expected to behave like non-porous SiOCH materials during the etching processes. In this work, the etch mechanisms of the hybrid material and the patterning of narrow trenches down to 50 nm using a metallic hard mask are studied. The etching is performed in an industrial capacitively discharge reactor using a fluorocarbon-based plasma. A parametric study on blanket wafers shows that the etch mechanisms are similar to those of a dense SiOCH material. However, surface analyses by XPS reveal that the higher carbon content in the hybrid material induced by the presence of porogen leads to the formation of a thicker fluorocarbon overlayer than with typical dense SiOCH materials. Consequently, the etching is very sensitive to the addition of polymerizing gas which can potentially lead to etch stop phenomena. The patterning of narrow trenches in hybrid materials shows that etch profiles are similar than in dense SiOCH layers. The main issue is the profile distortion induced by etch products redeposition on the trench sidewalls. XPS analyses are also conducted on the bottom and sidewalls of the trenches using the chemical topography analysis technique. The selectivity to the underneath etch stop layer (SiC) remains low (of about 4) indicating that the use and the development of a specific over etch step is required.

3:40pm **PS2-TuA6 Profile Control and Sidewall Modifications of Narrow Porous ULK Trenches after Plasma Etching and Pore Sealing Treatments***, **M. Darnon**, T. Chevolleau,* CNRS-LTM-France, France*; D. Eon,* CNRS-LTM-France*; F. Bailly,* CNRS-IMN-France, France*; L. Vallier,* CNRS-LTM-France*; J. Torres,* STM-France*; O. Joubert,* CNRS-LTM-France, France

In CMOS technology, for most of the interlayer dielectric materials, low k values are obtained by introducing porosity in order to reduce the total resistance capacitance delay in the interconnect levels. Trench or via patterns are currently transferred into porous SiOCH (p-SiOCH) using a dual hard mask strategy. In this work, we have investigated the profile control in narrow trenches etched using a metallic hard mask, and the characterization of the dielectric material degradation induced by the etching and pore sealing processes. The stack investigated is composed of 600 nm p-SiOCH, 40 nm SiO@sub 2@, 45 nm TiN and 100 nm photoresist (PR). The 200 mm wafers are patterned using direct ebeam lithography to achieve aggressive trenches dimensions down to 50 nm. The etching of p-SiOCH trenches is performed in a Magnetically Enhanced Reactive Ion Etcher (MERIE) using fluorocarbon gas mixtures. Pore sealing treatments on the patterned structures are achieved in a CH@sub 4@ or NH@sub 3@ plasma. Trenches profiles are observed by Scanning Electron Microscopy (SEM). Sidewalls and bottom surface composition are determined using chemical topography analysis by X-ray Photoelectron Spectroscopy (XPS). A parametric study reveals that profile distortions are attributed to by-products redeposition and hard mask faceting. The by-products redeposition is minimized by increasing the wafer temperature and/or using low polymerizing chemistries. The faceting is strongly reduced by lowering the ion bombardment. Whatever the etching conditions, the porous materials are modified on the trenches sidewalls. After narrow trenches etching with the optimized etch conditions, the impact of the pore sealing plasma treatments on the sidewalls and bottom modification is investigated. XPS analyses reveal that the pore sealing is attributed to the formation of a carbon rich layer with CH@sub 4@ plasma or a SiO@sub x@ layer with NH@sub 3@ plasma.

4:00pm **PS2-TuA7 Three-Dimensional Control of Interconnect Features: Sidewall Roughness Transfer During Patterning Processes***, **T. David**,* CEA-LETI-France, France*; J. Foucher, N. Posseme, A. Jacquier, A.-L. Fabre,* CEA-LETI-France

Dimensional control is a key challenge for present and future interconnect technology generations. The dominant architecture, damascene, requires tight control of patterning. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. For advanced nodes, feature size effects, such as electron surface scattering, will increase the effective resistivity and may require new technological development. Indeed characterization shows significant contributions to resistivity by scattering from both grain boundaries and sidewall patterns. In this work, we investigate the sidewall roughness (LWR, LER) transfer during interconnect patterning. The roughness is first calculated by performing threshold analysis of top down SEM images. However this technique does not take into account variations along feature height. Therefore, we have used a new 3D CD-AFM (Dimension X-3D) which enables us to characterize roughness along the features after each technological step of C065 etching processes on 300mm wafers. Trenches with various dimensions are patterned with conventional ArF photoresist. Then, the patterns are transferred into a metallic hard mask before etching of capping and dielectric layers. First results show a decrease of LWR during lithography pattern transfer into the metallic hard mask. Moreover LWR stays constant along profile height during capping and dielectric etching. Regarding LER, it seems that a slight increase is observed when going from the dense dielectric material (capping layer) to the more porous one (dielectric layer) while keeping LWR constant.

4:20pm **PS2-TuA8 Dry Etch Process of Contact holes using Multi-Functional Hard Mask***, **W.K. Kim**,* Hynix, Korea*; S.K. Lee,* Hynix, Korea, Republic of Korea*; J.H. Cho, J.H. Sun, K.L. Lee, G.S. Lee, S.C. Moon, J.W. Kim,* Hynix, Korea

As feature size continuously shrinks, pattern collapse has dramatically increased, which has led to decrease photoresist thickness and use hard mask materials as a pattern transfer layer. Amorphous carbon (a-C) is expected to be used in the nano technology regime because of its strong merits such as superior etching durability and low damage during strip. However it is not cost effective and complex in dry etching process. To overcome these problems, many of researchers focus on the new material development. Multi-functional hard mask (MFHM) is very useful in terms of cost reduction and process simplicity compared to a-carbon process. We call Si-ARC as a MFHM because it has to have both functions of anti-reflective and pattern transfer layer. We have evaluated the reactive ion etching characteristic of MFHM on spin-on carbon (SOC). In this study, we planned to form very fine pattern semiconductor of sub-80nm technology and beyond in combination of N_2/O_2 or N_2/H_2 without additional etching gas. The stack tested in this study was a Photoresist (100-150nm) / MFHM (100-200nm) / SOC (500-800nm) on insulator film (~2500nm). We focused on investigating etch rate, etch selectivity and etch profile. These are highly dependant to the polymer types of MFHM, SOC grain size, and Si content in MFHM. We also found that MFHM having Si-O-Si bond showed higher etch selectivity than that having Si-Si-O bond if their Si content is same. The small grain size in SOC and high Si content in MFHM are required to get better selectivity and profile. Especially, we obtained vertical fine pattern contact holes with minimized bowed profile by using N_2/O_2 plasma only and by partially oxidizing MFHM to SiO_2-like surface (SiON layer in case of a-C process). We confirmed the surface of MFHM was oxidized about 10~50nm in depth during etching process using AES, XPS, and TEM observation

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