Plasma Science and Technology
Room 2011 - Session PS2-MoM

Advanced Gate Fabrication

Moderator: E.V. Barnat, Sandia National Laboratories

8:00am **PS2-MoM1 Plasma Etch Challenges in Non-Planar Device Fabrication**, ***U. Shah***, *R.B. Turkot, Jr, T. Ghosh, S. Shankar,* Intel Corporation

As transistor development embraces multi-gate devices, new requirements are being placed on the patterning of these new structures. This paper discusses the challenges surrounding plasma etching of non-planar poly silicon gate electrodes required for multi-gate transistor development. The variation in type of structures, underlying materials and aspect ratios will be discussed. Some of the most common problems pertaining to etch processes of traditional planar devices such as gate profiles, notching, charge-induced damage of underlying material and selectivity requirements will be compared and contrasted between planar and non-planar geometries. Simulation results and models of how topography and underlying materials affects gate evolution and methods to control them will also be presented. Current metrology options used to characterize gate patterning and their inherent limitations will also be discussed in this paper.

8:20am **PS2-MoM2 Effect of Photoresist Trimming and Plasma Treatments on Line Roughness, Necking, and Bending During High Density Plasma Polysilicon Gate Etching**, ***S.A. Vitale***, *B.A. Smith, J.W. Blatchford, B.M. Rathsack,* Texas Instruments

Control of the polysilicon gate electrode length during high density plasma etching is one of the most challenging aspects of transistor fabrication at the 45nm technology node. According to the 2005 International Technology Roadmap for Semiconductors, the polysilicon gate length will be as small as 23nm for high performance microprocessors by 2008. Although transistor gate length has been shrinking by approximately 0.7x every 2 years, the line edge roughness has not scaled by the same factor. As a result, line edge roughness now can be as high as 25% of the gate length, resulting in severe degradation of transistor performance. In addition, systematic variations such as line necking and bending can result in line breakage and ultimately failure of the device. Solutions to reduce polysilicon gate line edge roughness, necking, and bending are critical to enable transistor performance and process yield at the 45nm node. In this work, high frequency line edge roughness of etched polysilicon gates is shown to originate primarily from roughness in the incoming photoresist. Plasma treatment to reduce the gate linewidth, commonly called plasma resist trimming, is shown to reduce the high frequency edge roughness. Line necking and bending, on the other hand, increases during the plasma resist trimming. AFM analysis of photoresist lines shows that torquing stresses during plasma resist trim is a primary factor in polysilicon gate bending and breakage. In general, high frequency line edge roughness is shown to be uncorrelated between the left and right edges of the lines. The effect of resist trimming and plasma treatments on the frequency spectrum of the roughness is also presented. HBr plasma curing, which can be used to harden photoresist and improve selectivity during polysilicon etch, is shown to neither improve nor degrade line edge roughness. Increasing oxygen concentration during the plasma resist trim step can be used to reduce line necking, at a given gate linewidth.

8:40am **PS2-MoM3 Understanding the Impact of Chamber Walls during Plasma Etching: a Key to Control Plasma Processes In ULSI**, ***R. Ramos***[1], Freescale Semiconductor, France*; G. Cunge, O. Joubert,* Laboratoire des Technologies de la Microelectronique, CNRS-LTM, France*; M. Orlowski,* Freescale Semiconductor, France*; T. Lill,* Applied Materials

Decrease in device dimension for integrated circuit manufacturing is challenged by wafer-to-wafer repeatability during plasma etching processes. Today's strategy to minimize potential drifts during plasma processes is to dry-clean the walls of the plasma chamber with an appropriate chemistry between each wafer to efficiently remove the etch products that have been deposited during the etch process. By using a simple technique that can monitor the chamber walls coating (based on X-ray Photoelectron Spectroscopy analyses) we have investigated the deposits formed on the chamber walls after metal / high-k (TiN, TaN, TaC, WSi@sub x@, HfO@sub 2@) gate etching processes, and the associated reactor cleaning strategies. We show that, in the most typical etch and clean processes, chamber walls are inevitably exposed to F-based plasma leading to the formation of AlF@sub x@ residues on the Al@sub 2@O@sub 3@ chamber walls. Sputtering of F atoms and AlF@sub x@ particles from this fluoride layer during the etching process then leads to uncontrolled concentrations of fluorine-based species and metal particles in the plasma gas phase that have an impact on the reliability of the process. We thus have investigated two potential solutions to overcome this issue without changing chamber walls material (for expensive Y@sub 2@O@sub 3@ liners for example): (1) dry-cleaning of AlF@sub x@ residues between each wafer, and (2) protecting the inner parts of the chamber walls with a thin coating before processing any wafer to provide a F-free, reproducible chamber environment. By comparing SiOCl coatings and carbon-rich coatings, we conclude that the latter ensures both better reproducibility and longer chamber walls lifetime, since reactor walls are never exposed to fluorine-based plasmas, therefore preventing AlF formation. Furthermore TEM picture shows that carbon-coated walls exhibit excellent capabilities for advanced gate stack patterning.

9:00am **PS2-MoM4 Effect of Etching Process on Gate LER**, ***A. Yabata***, *O. Koike, J. Hashimoto, I. Kurachi,* Miyagi Oki Electric Co., Ltd., Japan

In nano-scaled regime of semiconductor devices, effect of gate process on MOSFET is getting large. Especially for etching performance, shrinking technique and stable uniformity length are strictly required. In addition to them, reduction in LER (Line Edge Roughness) is very important too. It is the most critical issue for variability of current status and off stage leakage. Therefore, LER must be reduced for improving MOSFET. In widely study, LER is well known being large in 193nm ArF lithography and has poor durability for etching plasma exposure. But effect of another process parameter is not enough understood yet. In this paper, we focused on gate etching process and gate electrode material,and found new mechanism of gate LER formation.@footnote 1@ LER was evaluated by 3D AFM(Atomic Force Microscope) with sample of PR/BARC/PolySi/Oxide/Si sub. 3D AFM is directly measurement system of sidewall roughness with flared type tip. Firstly, effect of PR/BARC LER on gate LER was evaluated. PR/BARC LER was controlled by changing BARC etching gas chemistry. From the result, gate LER did not change at all without effect of drastic PR/BARC LER change. That indicates gate electrode LER must not be influenced by LER of masking layer. Secondary, the parameter of PolySi gate etching condition was focused. Dependence of pressure, source power, bias power and stage temperature were evaluated. From the result, effective parameter was only bias power and Gate LER was improved with increasing of bias power. That indicates LER has closely related with etching sputtering effect. Finally, we focus on effect of gate electrode material itself. It was was evaluated by surface roughness of PolySi. It was controlled by phosphorus dope method,concentration and anneal condition. From the result, gate LER was closely related with surface roughness. Therefore, gate electrode material is a key factor of LER formation. @FootnoteText@ @footnote 1@A.Yabata,et.al.:ICRP-6/SPP-23(2006) P-2A-30 451.

9:20am **PS2-MoM5 Plasma Atomic Layer Etching Using Conventional Plasma Equipment***, ***A. Agarwal***, University of Illinois at Urbana-Champaign*; M.J. Kushner,* Iowa State University

The thinning of the dielectric in gate stacks and the need to resolve etching on an atomic layer basis in applications such as FinFETs present large technological challenges in plasma etching. To insure atomic-level control it is desirable to use a self-limiting process which is independent of the processing time. In plasma atomic layer etching (PALE), formation of a monolayer of reactants or passivation is followed by the removal of the layer that then self terminates the process. For example, deposition of a thin layer of polymer or passivation in a non-etching plasma followed by etching in a non-polymerizing plasma with low energy ion energy could remove only a single layer or less of underlying material. The higher threshold energy required to remove the underlying material in the absence of the passivation would self-terminate the process. A challenge is to perform these processes in conventional plasma equipment as opposed to highly specialized beam equipment. In this talk, results from a computational investigation of PALE will be discussed with the goal of demonstrating the potential of the process using conventional etching tools. The Hybrid Plasma Equipment Model (HPEM) and the Monte Carlo Feature Profile Model (MCFPM) were modified to have pulse periodic capability as required for PALE, and to kinetically resolve ion energy distributions to finely resolve threshold energies. Results for PALE will be discussed, for geometries of interest to future technological nodes, for at least two systems: 1) PALE of Si using steps of an Ar/Cl@sub 2@ plasma (passivation) followed by Ar plasma (etch) and 2) PALE of SiO@sub 2@ using steps of a fluorocarbon plasma (passivation) followed by an Ar

[1] **PSTD Coburn-Winters Student Award Finalist**

plasma (etch). @FootnoteText@ *Work supported by Semiconductor Research Corp. and the National Science Foundation.

9:40am **PS2-MoM6 Impact of Plasma Damage on Cobalt Silicidation**, ***T. Kimura***, *K. Kugimiya, K. Fuke, T. Ohchi, T. Kataoka, T. Tatsumi, Y. Kamide,* Sony Corporation, Japan

Silicides must be introduced to ULSI circuits to improve sheet and contact resistance. Generally, silicidation on the source and drain depends strongly on the surface, so controlling damage to the silicon substrate from sidewall etching is very important. We studied sidewall etching using a capacitive coupled plasma type etcher. RF power supplies with different frequencies (2 and 13.56 MHz) were used for the lower electrode. The thickness of the damage layer in the silicon surface resulting from sidewall etching was conveniently evaluated by ellipsometry. As Vpp is increasing, the thickness of the damage layer is increasing in the case of sidewall etching with CH@sub 2@F@sub 2@ gas chemistry and the thickness is decreasing in the case of etching with a RF power supply of higher frequency under conditions where the same Vpp was obtained. We calculated the ion energy distribution function. The thickness of the damage layer has a clear relationship to ion energy at the high energy peaks for both frequencies. The damage thickness also depends on gas chemistry. When we used the CF@sub 4@ plasma, the thickness of the damage layer was thinner than that induced by the CH@sub 2@F@sub 2@ plasma and did not seem to depend on RF bias power. This is presumably due to the absence of H ions, which can penetrate Si more deeply. We could successfully form conformal CoSi@sub x@ on the source and drain after sidewall etching with CF@sub 4@ gas chemistry, but we could not after etching with CH@sub 2@F@sub 2@ gas chemistry. For mass production to occur, high quality CoSi@sub x@ must be formed to create 32-nm devices and the control of ion energy distribution in the dry etching system must be improved.

10:20am **PS2-MoM8 Plasma Etching Challenges of New Materials Involved in Gate Stack Patterning for sub 45 nm Technological Nodes**, ***O. Joubert***, CNRS-LTM-France, France*; A. Le Gouil,* STM-France*; R. Ramos,* CNRS-LTM-France*; M. Helot,* STM-France*; O. Luere, E. Richard,* CNRS-LTM-France*; G. Cunge, T. Chevolleau,* CNRS-LTM-France, France*; E. Pargon, L. Vallier,* CNRS-LTM-France*; T. Morel,* CEA-LETI-France*; S. Barnola,* CEA-LETI-France, France*; T. Lill, J.P. Holland, A. Patterson,* AMAT-USA **INVITED**

In plasma etching processes, the complexity comes from the introduction of new materials and from the reduction in dimension of the structures involved in CMOS devices. In the gate stack patterning step, the precision of the critical dimension (CD) control required to pattern silicon gates on thin SiON dielectrics has required an unprecedented effort of the etch community to design all the plasma etching steps allowing a CD control better than 3 nm across a 300 mm wafers. The introduction of metal layers and high K dielectric materials in the sub 45 nm gate stack is even more challenging since time and experience are missing to reach the degree of control required to fabricate such complex stacks in a range of dimension between 20-30 nm. In this presentation, we will show what new issues are faced when a metal layer is introduced in the gate stack: etch chemistry compatibility between silicon and metal (strongly metal dependent), profile deformation of the silicon top part of the gate when etching the thin metal layer, process strategy (etch silicon and metal in one step or in two steps), impact of chamber wall coatings on profile control and selectivity issues between metal and high K. The etching of high K HfO@sub 2@ based materials is also complex. First, after metal etching, the thin high K layer has been modified (covered by significant concentrations of halogens, roughness). Furthermore, the thin high K layer must be removed without generating damage in the underlying silicon and without generating profile deformation of the top part of the gate. All the issues will be discussed by showing the practical integration of TiN, TaN, WN, W in advanced gate stacks and discussing our results with the support of powerful in situ characterization techniques such as chemical topography analyses using XPS, mass spectrometry, as well as TEM and SEM cross sections.

11:00am **PS2-MoM10 Ta and Mo-based Metal Etch for Advanced Gate Stacks**, ***E. Luckowski***, *A. Martinez, S. Rauf,* Freescale Semiconductor, Inc.

The continued scaling of conventional CMOS devices becomes increasing difficult due to the additional series capacitance caused by polysilicon depletion, which decreases gate capacitance and requires increasingly thin gate dielectric layers. High-K dielectrics in conjunction with polysilcon gates address this problem, but interactions between polysilicon and gate dielectric material make implementation of this solution difficult. An increasingly attractive solution to these problems is the use of metal electrodes with suitable work functions and sufficient physical and electrical stability. Because selection appropriate gate electrode is driven mainly by the work function of the metal, these materials pose significant challenges that require an in-depth understanding of plasma etch properties and mechanisms in order to successfully fabricate aggressive dimensions of current advanced gate stack devices. In this work we investigate the impact of plasma parameters on etching characteristics of Ta and Mo-based materials for advanced gate stack device applications. In particular, etch rates and selectivites are discussed with respect to fabricating single and dual metal gate CMOS structures. The impact of metal etch processes on polysilicon and high-k dielectric layers will also be discussed. OES and in-situ reflectometry are used to characterize composition and changes in the plasma conditions, etch rates and profiles measured by four point probe, XRR, SEM and TEM. Plasma modeling is also done using a 2D integrated equipment-feature scale model to improve understanding of the mechanisms of metal gate etch processes.

11:20am **PS2-MoM11 Influence of Stopping Layer Nature on Poly-Si/Metal Gate Patterning Process**, ***V. Paraschiv***, *D. Shamiryan, M. Demand, S. Beckx,* IMEC, Belgium*; C.G.N. Lee, G. Kota,* LAM Research*; W. Boullart,* IMEC, Belgium

TiN or TaN layers are introduced between poly-Si electrode and the gate dielectric to solve the poly-Si depletion and boron diffusion issues. Although a minimal change is introduced we show that this modification has a significant impact on poly-Si etch due to the nature of the layer underneath the poly-Si electrode (dielectric or metallic). The etch was carried out in a Lam Research Versys2300 etch reactor. Poly-Si gate etch includes main etch (ME), soft landing (SL) and over etch (OE).@footnote 1@ SL is critical since it has to stop on SiO2 and has to keep a straight gate profile. For conventional (poly-Si/SiO2) gate stack the etch time after end point (EP), during SL, defines the bottom profile since the SiO2 starts accumulating positive charges inducing ions deflection at the bottom of the gate.@footnote 2@ The deflected ions remove the poly-Si foot present at the moment of EP. Conventional gate etch could not remove the poly-Si foot when stopping on metal, apparently due to lack of charge accumulation and the corresponding ion deflection. Although, the metallic layer can be oxidized by O2 present in the SL etch chemistry, the bottom power required for ion deflection is too low and results in damaging the top gate profile, due to hard mask charging effect (negatively charged oxide hard mask deflects ions distorting gate profile).@footnote 3@ Changing the ME chemistry from HBr/Cl2/CF4/O2 to SF6/CH2F2/N2 provides better passivation of poly-Si sidewalls allowing a SL step with a very low bottom power (65V) that removes the poly-Si foot without affecting the top profile. Although both TiN and TaN are conductive, it is more difficult to remove the poly-Si foot when stopping on TiN due to their different oxidation behavior. @FootnoteText@ @footnote 1@ E. Pargon et al., J. Vac. Sci. Technol. B 23(5), 1913 (2005).@footnote 2@ G. S. Hwang et al., J. Vac. Sci. Technol. B. 15, 70 (1997).@footnote 3@ D. Shamiryan et al., J. Vac. Sci. Technol. B, 23 2194 (2005).

11:40am **PS2-MoM12 Plasma Etching of Tungsten Nitride for sub 45nm Metal Gate**, ***S. Barnola***, CEA-LETI/France, France*; T. Morel,* STMicroelectronics

With the reduction of the CMOS devices dimensions on standard poly-silicon gates, the poly depletion effect is a major problem to achieve low equivalent oxide thickness. Inserting a well chosen metal layer between the poly-silicon and the dielectric is one of the solutions, which transform a pure silicon gate into a metal gate where the work function of the metal layer is a key factor The use of thin MOCVD tungsten nitride layers (10nm) to achieve the PMOS devices on 300mm wafers is pretty novel. Its integration into a complete gate stack (Poly-Si/TiN/WN/SiO@sub 2@ or highK) is quite challenging in terms of dry etch. In this work we focused on understanding the etch mechanisms of tungsten nitride in chlorine and fluorine based chemistries on a 300mm ICP tool, with in-situ optical emission spectroscopy and in-situ interferometer. We investigated the selectivity over several dielectrics (SiO@sub 2@ and Hafnium based material) on blanket wafers. Chemical analysis of the interaction layers were performed by X-ray Photoelectron Spectroscopy (XPS) on the involved materials. High selectivity numbers (@>=@50:1) were easier obtained on Hafnium based dielectric than on SiO@sub 2@, especially in fluorine based chemistries with the low volatility of the hafnium by products. Nevertheless, good enough selectivity numbers were also achieved on SiO@sub 2@ in fluorine chemistry at low bias voltage. The integration of the WN etch into a multiple steps process for sub 45nm metal gates was investigated in terms of CD & profile control by Scanning Electron Microscopy (SEM).

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