Plasma Science and Technology
Room 2009 - Session PS1-ThA

Plasma Processing for High-K/III-V's and Smart Materials

Moderator: J. Margot, Université de Montréal, Canada

2:00pm **PS1-ThA1 Mechanisms and Selectivity for Etching of HfO@sub 2@ and Si in BCl@sub 3@ Plasmas**, ***C. Wang***, *V.M. Donnelly,* University of Houston

We have investigated etching of HfO@sub 2@ and poly-Si in BCl@sub 3@ plasmas as a function of substrate temperature (T@sub s@), source power, and substrate bias. The etching rates of both HfO@sub 2@ and poly-Si increase with increasing T@sub s@. An activation energy of 4.7 kJ/mol is obtained from an Arrhenius plot of HfO@sub 2@ etching rate vs. T@sub s@. This activation energy is much lower than the heat of vaporization of HfCl@sub 4@ (100 kJ/mol), hence desorption of this product is not rate limiting. The most likely mechanism is one in which the surface, disordered by ion bombardment, is terminated with Hf-O-BCl@sub 2@ and Hf-Cl groups. Etching is limited by chemical sputtering of this chemisorbed layer. Higher T@sub s@ modestly increases the rate at which reactions occur during ion "thermal" spikes. Similarly, the desorption of SiCl@sub 4@ is not limited by the vapor pressure of this product, which is orders of magnitude higher. The etching rate of Si in BCl@sub 3@ plasmas has an activation energy of 3±1 kJ/mol. Consequently, a small improvement in HfO@sub 2@ selectivity over Si can be realized at high temperature. At high (inductively coupled) power, a relatively thin BCl@sub x@ film (detected by vacuum-transfer to an XPS chamber) forms on partially etched HfO@sub 2@ and Si. At low (capacitively-coupled) power, a similar thickness films is present on HfO@sub 2@, but a much thicker BCl@sub x@ film is present on Si. BCl@sub 3@ dissociates in the plasma to yield Cl and BCl@sub 2@ at low power, and additionally, BCl, B, and Cl at high power. Apparently, the rate of BCl@sub x@ deposition on Si does not increase, or increases less than the rate of etching of Si as power increases, perhaps due to a lower sticking coefficient of BCl, compared to BCl@sub 2@, and the enhanced Cl flux. The BCl@sub x@ film formed on the Si surface likely inhibits the formation and sputtering of volatile SiCl@sub x@ species. Supported by SRC and AMD Inc.

2:20pm **PS1-ThA2 Plasma Etching of HfO2 in High-Density Chlorine-Containing Plasmas without RF Biasing**, ***K. Nakamura***, *K. Osari, D. Hamada, K. Eriguchi, K. Ono,* Kyoto University, Japan

As ultra large scale integrated circuit dimensions continue to be scaled down, high dielectric constant (high-k) materials such as HfO@sub 2@, ZrO@sub 2@, and Al@sub 2@O@sub 3@ are being required as gate dielectric to maintain the gate capacitance in smaller size. For the fabrication of high-k gate stacks, a better understanding of the etching characteristics and mechanisms is indispensable for high-k dielectrics. We have investigated the etching of high-k materials of HfO@sub 2@ using high-density chlorine-containing plasmas excited by electron cyclotron resonance. Experiments were performed in BCl@sub 3@/Cl@sub 2@ gas mixtures at a pressure of 5 mTorr without rf biasing. In pure BCl@sub3@ plasma, some deposition was found to occur on HfO@sub 2@ surface to inhibit etching. By adding Cl@sub 2@ to BCl@sub 3@, the deposition was suppressed to result in etching of HfO@sub 2@. The HfO@sub 2@ etch rates increased with increasing Cl@sub 2@ concentration ratio, and the maximum HfO@sub 2@ etch rate was ~100 nm/min at 60% Cl@sub 2@ addition. At the Cl@sub 2@ concentration ratio in the range 25-50%, the HfO@sub 2@ etch rate was more than 20 nm/min, while the Si etch rate remained almost zero, thus giving extremely high selectivity over Si. In addition, by adding a small amount of O@sub 2@ to BCl@sub3@/Cl@sub 2@, the HfO@sub 2@ etch rate was further enhanced. The maximum HfO@sub 2@ etch rate was ~150 nm/min at 5% O@sub 2@ addition to BCl@sub 3@/60%-Cl@sub 2@ plasma, while the Si etch rate also increased to deteriorate the selectivity over Si down to 4. These results were compared with plasma and surface diagnostics, to understand plasma-surface reaction mechanisms responsible for selective etching of HfO@sub 2@.

2:40pm **PS1-ThA3 Effects of Low Energy Nitrogen Plasma on the Removal of HfSiON**, ***W.S. Hwang***, National University of Singapore*; W.J. Yoo,* Sungkyunkwan University, Korea, Singapore*; B.J. Cho, D.S.H. Chan,* National University of Singapore

HfSiON high-k dielectric is being studied extensively to improve the electrical properties of conventional SiON dielectric since it can attain low leakage current especially for low standby power application. The removal of high-k dielectric using a wet etching technique is more frequently used than dry etching techniques which result in poor etching selectivity over underlying Si. Dilute hydrofluoric acid (DHF) solution etches amorphous HfSiON easily without the loss of the underlying Si. However, crystallized HfSiON shows strong resistance in DHF after post-deposition anneal, posing challenges in the integration involving the removal of high-k dielectric at the active transistor regions of source and drain. In this work, the DHF wet removal of HfSiON assisted by N@sub 2@ ion bombardment is investigated. The anisotropic and undercut-free profile is achieved by this technique. An as-deposited amorphous HfSiON of 4 nm can be removed by 1% DHF in 15s, whereas the annealed crystallized HfSiON cannot be removed. N@sub 2@ plasma treatment helps the crystallized HfSiON to be etched in DHF. The ion assisted wet removal is made feasible via changing the structure of the crystallized HfSiON to the mixture of metallic Hf and amorphous HfSiON. We found a correlation between ion energy and formation energy of HfSiON; the ions having energy less than 9eV do not penetrate HfSiON, whereas ions having energy higher than its formation energy of ~ 9.3eV penetrate HfSiON and participate in the formation of SiN. The low energy ion assisted wet removal method results in lower threshold voltage than the conventional DHF wet etching method which causes lateral encroachment of HfSiON that lowers gate oxide capacitance. This plasma assisted method can be applied extensively to various removals of high-k material constrained by low crystallization temperature and thereby high etching resistance in conventional DHF.

3:00pm **PS1-ThA4 Vacuum-Ultraviolet Induced Photocurrents in Plasma-Charged, Atomic Layer Deposited, HfO2/SiO2/Si Dielectric Stacks***, ***G.S. Upadhyaya***, *J.L. Shohet,* University of Wisconsin-Madison

Advanced MOS technologies currently utilize gate oxides so thin that any further decrease in silicon-oxide thickness results in a large increase in power consumption due to high gate-leakage current. High-K dielectric materials are being investigated in order to maintain high coupling capacitance and limiting the leakage current by using thicker gate-oxide layers. In this work, we utilize the high-K dielectric hafnium oxide because of its resistance against silicide formation. It is well known that plasma and vacuum-ultraviolet (VUV) radiation-induced damage during fabrication adversely affects device reliability by degrading the gate oxide. The VUV-radiation response of hafnium oxide is relatively unknown. To this end, we investigate the effect of VUV radiation with energies from 7 to 21 eV, which is the range of energies emitted by most processing plasmas, on uncharged as well as plasma-charged, atomic-layer deposited (ALD) HfO2/SiO2/Si dielectric stacks. The electron-storage ring at the University of Wisconsin Synchrotron Radiation Center will be used as the VUV source. By measuring the substrate and photoemission currents during irradiation and the resulting surface potential, information about the nature of traps and rate of interface state generation in dielectric layers as a function of photon energy can be obtained. Comparison of HfO2 with SiO2 dielectric layers shows that, due to the lower bandgap of HfO2, traps and interface states in HfO2 are populated at a lower VUV photon energy than for silicon oxide. This indicates that charging of HfO2 during processing may occur more easily than for SiO2. @FootnoteText@ *Worksupported by the National Science Foundation under grant No. DMR-0306582. The UW-Synchrotron is a national facility, funded by the National Science Foundation under grant No. DMR-0084402.

3:20pm **PS1-ThA5 Mechanisms of Plasma-Induced Damage during Ion-Assisted Chemical Etching of Indium-Zinc-Oxide Films in Reactive Plasma Chemistries**, ***L. Stafford***, *W.T. Lim, S.J. Pearton,* University of Florida*; J.-I. Song, J.-S. Park, Y.W. Heo, J.-H. Lee, J.-J. Kim,* Kyungpook National University, Korea

Because of its good electrical conductivity, wide transmittance window, large work function, excellent surface smoothness, and low deposition temperature, Indium-Zinc-Oxide (IZO) has recently emerged as a very promising material for transparent electrodes in various optoelectronic devices such as liquid crystal displays, light-emitting-diodes, and solar cells. While the growth characteristics of IZO layers are relatively well optimized, the development of a reliable pattern transfer process remains to be examined. In this work, we investigate the potential of Cl@sub 2@ and CH@sub 4@/H@sub 2@ plasma chemistries for the dry etching of IZO films. The influence of the discharge chemistry on the post-etched surface morphology and near-surface stoichiometry is also investigated. While the Cl@sub 2@-based plasma shows little enhancement over physical sputtering in a pure argon atmosphere, the CH@sub 4@/H@sub 2@/Ar chemistry produces a strong increase of the IZO etch rate. The surface morphology of IZO films after etching in Ar and Ar/Cl@sub 2@ discharges is smooth, whereas that after etching in CH@sub 4@/H@sub 2@/Ar presents

particle-like features resulting from the preferential desorption of In- and O-containing products. While the etch-induced damage in Ar and Ar/Cl@sub 2@ plasmas are constrained to the surface vicinity, etching in CH@sub 4@/H@sub 2@/Ar produces a Zn-rich surface layer, whose thickness (~55 nm) is well-above the expected range of incident ions in the material (~1.5 nm). Auger electron spectroscopy measurements as a function of plasma exposure time indicate that diffusion of O, Zn and In atoms upon preferential desorption of volatile O- and In-containing reaction products is responsible for damage formation. A diffusion model accounting for the observed depth profiles is proposed. Such damage of the IZO layer is expected to have a significant impact on the transparent electrode properties in optoelectronic device fabrication.

3:40pm **PS1-ThA6 Reactive Plasma for High Aspect Ratio Etching and Surface Modification***, **S.W. Pang,*** The University of Michigan **INVITED**

In this talk, plasma etching of Si, GaAs, and polymer will be reviewed. Depending on the applications, fast etch rate, high aspect ratio etching, and damage-free etching are required. In Si and GaAs etching, fast etch rates have been demonstrated to produce vias by etching through an entire wafer. On the other hand, for devices with nanostructures, high aspect ratio (large height and narrow width) etching is needed to minimize lateral etching. In addition, for these devices to be electrically or optically functional, surface damage due to plasma etching has to be eliminated. Additionally, to remove polymer inside nanochannels of microfluidic systems, fast lateral etching of polymer has been developed. Etch conditions that can provide the desired etch characteristics will be discussed. Finally, surface energy of various materials could be modified by exposure to reactive plasmas. Results of applying plasma surface treatment to reversal nanoimprint will be shown.

4:20pm **PS1-ThA8 Atomic Layer Etching of III-V compounds using a Low Angle Forward Reflected Neutral Beam***, **S.D. Park**, C.K. Oh, J.W. Bae, G.Y. Yeom,* Sungkyunkwan University, Korea

III-V compounds are currently investigated for various electronic and optical devices, due to high electron mobility and high useful temperature range. Therefore, a few researchers have investigated on the dry etching of III-V compounds using halogen-based reactive-ion-etching (RIE). However, these conventional RIE processes lead to physically damage to the surface of the devices, such as creation of surface defect including structural disruption, intermixing layer or stoichiometry modification and the increment of surface roughness, due to the use of energetic reactive ions to achieve vertical etch profiles. Among those dry processes, atomic layer etching (ALET) can be assigned as the most possible method to realize atomic scale etch-rate controllability of III-V compounds without physically damaging to the surface of III-V compounds. In this study, the ALET of III-V compounds were carried out using a sequential Cl@sub 2@ adsorption and a Ne neutral beam irradiation to the surface. By supplying Cl@sub 2@ and Ne neutrals higher than critical doses, the exactly same etch depth per cycle corresponding to one atomic layer per cycle could be obtained by a self-limited etching mechanism. The etched step height was measured using a step profilometer. The measured step height was divided by the total number of ALET cycles to yield the etch rate per cycle. An atomic force microscope (AFM) was used to measure the surface roughness. Also, X-ray photoelectron spectroscopy (XPS) was utilized to analyze the change of composition of III-V compounds.

4:40pm **PS1-ThA9 Improvement of Programming Characteristics of Ge2Sb2Te5 Thin Films by Incorporating SiO2 for Application of PcRAM***, S.W. Ryu, **J.H. Oh**, B.J. Choi,* Seoul National University, Korea*; S.K. Hong,* Hynix Semiconductor Inc., Korea*; C.S. Hwang, H.J. Kim,* Seoul National University, Korea

In an effort to overcome the scaling limit of the floating gate non-volatile memory (NVM) technology below the 30nm design rule, the semiconductor industry has been forced to find alternative NVM.@footnote 1-4@ Phase change random access memory (PCRAM) attracts great interest not only because it satisfies the various demands for NVM devices but also because its fabrication process is relatively simple. However, the high level of reset current has been the major obstacle for further scaling of PCRAM because of the limited on-current drive capability of the cell transistor (<1mA/μm) and then unexpected crystallization of unstable amorphous state has resulted from low crystallization temperature of Ge @sub 2@Sb@sub 2@Te@sub 5@ (GST). The phase change characteristics of GST films for phase change random access memory devices were improved by incorporating SiO@sub 2@ into the GST film through co-sputtering at room temperature. Isochronal annealing showed an increased resistivity of the crystallized GST films in proportion to the incorporated quantity of SiO@sub 2@ which leads to a reduction in the writing current. Incorporated SiO@sub 2@ also inhibits crystallization of the amorphous GST film which can improve the long term stability of the meta-stable amorphous phase. @FootnoteText@ @footnote 1@S. Hudgens and B. Johnson, Mater. Res. Soc. Bull. November, 2002, p.829. @footnote 2@S. Lai, Tech. Dig. Int. Electron. Devices Meet. Washington, DC, 2003, p.255. @footnote 3@S.Y. Lee and K. Kim, Int. Conference on Integrated Circuit Design and Technology, 2004, p.45. @footnote 4@Y. N. Hwang, S. H. Lee, S.J. Ahn, S.Y. Lee, K.C. Ryoo, H.S. Hong, H.C. Koo, F. Yeung, J.H. Oh, H.J. Kim, W.C. Jeong, J.H. Park, H. Horri, Y.H. Ha, J.H. Yi, G.H. Koh, G.T. Jeong, H.S. Jeong and K. KiM, Tech. Dig. Int. Electron. Devices Meet. Washington, DC, 2003, p.893 .

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