Plasma Science and Technology
Room 2009 - Session PS1+MS+NM-TuM

Plasma Patterning

Moderator: A. Agarwal, University of Illinois at Urbana-Champaign

8:00am **PS1+MS+NM-TuM1 Resolving Gate Patterning Issues at sub 65 nm Technology Nodes***, **T.J. Kropewnicki**, C.-C. Fu,* Freescale Semiconductor, Inc.

According to the 2005 edition of the International Technology Roadmap for Semiconductors, the physical gate length of high performance transistors at the 65 nm technology node is expected to be 25 nm in 2007, decreasing to 18 nm at the 45 nm node in 2010. Clearly, these goals present a clear challenge to photolithography and etch, which together are responsible for resolving these features on wafers. In addition to the pure scaling aspects of technology progression are the many additional enhancements such as stressors, which are being used to push the performance of silicon circuits. In certain integration schemes, these stressors add complexity to the transistor gate stack and accelerate photoresist bending and line collapse which cause etch masking, and ultimately variable, uncontrollable line widths. This paper will begin with a brief description of the transistor module process flow, highlighting the new challenges introduced to the gate stack etch at sub 65nm technology nodes. Next, a combination of enhancements in the gate photolithography and etch steps used to address these challenges will be presented. Results from these experiments will show a 50% reduction in across wafer line width variation, and a near 100% reduction in the incidence of polysilicon pattern distortion. Finally, the possible mechanisms for the increased levels of polysilicon pattern distortion seen with advanced transistor modules will be discussed.

8:20am **PS1+MS+NM-TuM2 Plasma Impact on ArF Resist Line Edge Roughness***, **J. Thiault**,* LTM / CNRS France, France*; E. Pargon,* LTM / CNRS France*; J. Foucher,* CEA LETI France*; O. Joubert, G. Cunge,* LTM / CNRS France, France

As Critical Dimensions for semiconductor devices shrink too few tens of nanometers, the Line Edge Roughness (LER) or Line Width Roughness (LWR) becomes a critical issue because it can degrade resolution and linewidth accuracy that causes fluctuations of transistors performances. ArF resist patterns present a LWR of about 8 nm after lithography that is possibly transferred into the underlayers during plasma processing steps, resulting in a final LWR above the requirements of the International Technology Roadmap for Semiconductors (ITRS, which tolerates a LWR of around 3 nm for the 65nm technology node). In this study, isolated ArF resist patterns have been exposed to different plasma chemistries under identical processing conditions to investigate the impact of the plasma chemistry on the resist LWR. The sidewall roughness characterization has been performed using 3D Atomic Force Microscope (AFM3D) and top view Scanning Electron Microscope (CD-SEM). Experimental results tend to show that when the plasma/resist interaction is strongly chemically driven, such as in O@sub 2@ or SF@sub 6@ plasmas, with no bias applied to the wafer, the resist sidewalls are not smoothen. However, using plasma conditions where the ion bombardment component of the plasma is increased (by applying a bias power to the wafer), a LWR reduction is measured. This trend has been confirmed by exposing resist patterns to chemically inert plasmas such as Ar plasmas. Moreover, we have investigated plasma curing treatment on resist patterns, currently used in semiconductor manufacturing to reinforce the etching resistance of the resist. In this type of plasma (HBr based) where the ion current density is high and ion energy low, we also observe a decrease in LWR. All these trends suggest that the anisotropic ion flux is responsible for the smoothing of the resist sidewall roughness by eroding the bumps present on the resist sidewall.

8:40am **PS1+MS+NM-TuM3 ArF Resist Friendly Etching Technology***, **T. Hayashi**, Y. Morikawa, K. Suu,* ULVAC Inc., Japan **INVITED**

The requirements for dry etching technology in semiconductor processes beyond 90 nm node come to be very complicated and difficult. In photolithography, the introduction of ArF resist has started. ArF resists generally have very weak plasma resistance and are deformed in the etching process. However, as for the fundamental mechanism of deformation of resists in dry etching, sufficient discussions have not been done yet. So far ArF resist deformation has been thought to be caused by ion impinging damage. However, in our experiments, the deformation was not found in the high density NLD plasma in lower pressure than 1Pa, which gives relatively higher ion flux to the surface. So if ion energy is the main origin of the ArF resist deformation, then the NLD plasma might give a large resist deformation. Contrary to this expectation, however, the etched profiles in the NLD plasma showed low line edge roughness and almost nothing of striation. Considering these facts, the ArF resist deformation is clearly caused by concerted working of ion impinging damage and subsequent radical reactions at the resist-damaged area. This means if either of ion damage or radical reaction is nothing then the ArF resist deformation is nothing or is suppressed considerably lower. Therefore, the lower pressure process below 1 Pa or the lower reactive radical density process is necessitated. The latter is achieved by using highly effective radical scavenger. Generally H or CO has been used as the scavenger of F atoms. However, Br and I may be more effective as the scavenger, because Br and I react with F atoms and form stable inter-halogen compounds. So use of iodine or bromine contained perfluoro-hydrocarbon compounds like CF3I gives the ArF resist friendly etching process. Actually very smooth etched surfaces were obtained for patterned ArF resist/ARC/CAP/low-k/BARC/Si wafers. This work was partly supported by NEDO (New Energy and Industrial Technology Development Organization) in Japan.

9:20am **PS1+MS+NM-TuM5 Plasma Etching of Nano-Scale, Sub-10nm, Features***, **Y. Zhang**, C.T. Black, H.-C. Kim, E.M. Sikorski, T. Dalton,* IBM Research

Features Patterning nano-scale semiconductor features with precision imposes many new challenges for plasma etching. One of the challenges is that as the sizes of nano-scale features shrinking down to the sub-10nm regime, Plasma etching seems to approach to the limits. In this paper, we report the recent results of studying plasma etching of true nano-scale features using tow kinds of nano-sacle patterns. The first type of samples is diblock copolymer (similar to resist) self assembled nano holes and lines. The second kind samples are self-assembled organosilicate (similar to silicon oxide) nano patterns. With samples pattern, arrays of nano holes or nano lines' dimensions in the range of ~10nm, we studied plasma etching challenges for transferring nano-scale patterns into different materials (silicon, and silicon dioxide) in different plasma chemistries and process conditions. By varying the thickness of masks, the characteristics of aspect ratio dependence vs. "real" etching limits due to the sizes of sub-10nm nano-scale features were studied. The impacts of mask selectivity and line edge roughness (LER) to transferring sub-10nm patterns will be also discussed.

9:40am **PS1+MS+NM-TuM6 Nickel Atom and Ion Density in an Inductively Coupled Plasma with an Internal Coil***, **L. Xu**[1],* University of Houston*; N. Sadeghi,* University Joseph Fourier-Grenoble & CNRS, France*; M.K. Jain, S.C. Vemula, V.M. Donnelly, D.J. Economou, P. Ruchhoeft,* University of Houston

Nanopantography uses monoenergetic ion beams to enable massively parallel patterning of nano-sized features (e.g. 10 nm dia., 100 nm deep holes etched into Si). Deposition of metal nanodots (e.g. Ni) can have applications such as catalysts for the growth of an orderly array of carbon nanotubes. For this purpose, we have developed an inductive plasma source containing a relatively large fraction of Ni@super +@. A two-turn Ni coil immersed in the plasma generates a Ni-containing Ar plasma. Ni was sputtered both from the negatively self-biased coil and from a Ni target powered by a separate rf power. By adding a trace amount of N@sub 2@, gas temperatures T@sub g@ (= rotational temperatures) were derived from N@sub 2@(C-B) spectra. At low powers (capacitively coupled), T@sub g@ derived from the 0-0 band was erroneously high. This was attributed to energy transfer from Ar metastable atoms to the N@sub 2@ C (@upsilon@=0). At high powers (inductively coupled), both the N@sub 2@ 0-0 and 4-4 bands provided the same reasonable T@sub g@ because electron-impact dominates excitation at high power. Optical emission of Ar at 419.8 nm was used to estimate the plasma density, and was in agreement with values predicted from a global model. Ni densities were determined by optical absorption (using a Ni hollow cathode lamp) and were found to increase with pressure and power. The Ni@super +@ densities also increase at higher pressures and powers. Model predictions of Ni@super +@ densities are consistent with metastable Ni@super +@ densities derived from optical absorption. Finally, 50nm dia. Ni islands have been deposited in preliminary nanopantography experiments with the Ni@super +@ beam.

[1] **PSTD Coburn-Winters Student Award Finalist**

10:40am **PS1+MS+NM-TuM9 Bias Frequency Effect on SOC Film Degradation in sub-45 nm Line and Space Pattern SiO@sub 2@ RIE using S-MAP**, ***H. Hayashi***, *K. Kikutani, J. Abe, A. Kojima, T. Oohashi, I. Sakai, T. Ohiwa,* Toshiba Corporation, Japan

Sub-45 nm line and space pattern etching of SiO@sub 2@ film was studied using a stacked mask process (S-MAP) which consists of photoresist, spin-on-glass (SOG) and spun-on-carbon (SOC) film stacked structure. Maintaining pattern integrity becomes more challenging with the decrease of pattern size. Reduction of the hydrogen content of SOC, suppressed the fluorination reaction of its C-H bonds during SiO@sub 2@ etching which lead to line pattern wiggling, and as a result, 56 nm line and space pattern etching was realized.@footnote 1@ This time, the effect of ion energy distribution on SOC degradation in the SiO@sub 2@ etch process was investigated for sub-45 nm line and space pattern etching. The ion energy distribution was varied by dual frequency superimposed (DFS) RIE, using the conditions of 100 MHz rf supply with 3.2 MHz superimposed compared with 100 MHz with 13.56 MHz superimposed. The other SiO@sub 2@ etch conditions were the same, that is, C@sub 4@F@sub 8@ gas chemistry with the same electron density and self-bias voltage (-Vdc) of 6x10@super 10@ cm@super -3@ and 350 V, respectively. As a result, SOC line pattern wiggling was observed in the 3.2 MHz case, but it was suppressed in the 13.56 MHz case, even though the SiO@sub 2@ etch rates were 241 nm/min and 254 nm/min, respectively, and about the same. This shows that, by using DFS RIE with 13.56 MHz superimposed, SOC degradation can be suppressed while maintaining the SiO@sub 2@ etch rate for sub-45 nm line and space pattern etching. The maximum ion energy in the 13.56 MHz case should be lower than that of the 3.2 MHz case under the same -Vdc conditions, because with higher rf frequency, it would have a narrower ion energy distribution. In this way, SOC degradation was suppressed without decrease of the SiO@sub 2@ etch rate. In conclusion, S-MAP combined with 100 MHz/13.56 MHz DFS RIE realized sub-45 nm line and space pattern SiO@sub 2@ etching. @FootnoteText@ @footnote 1@ J. Abe et al., Symp. Dry Process, (2005) 11.

11:00am **PS1+MS+NM-TuM10 High Aspect Ratio (>10:1) Amorphous Carbon Layer Etching Using Soft Etch Capability in a High Frequency Capacitive Coupled Plasma Source Dielectric Etch Chamber**, ***S. Sung***, *J. Wang, S. Ma,* Applied Materials

Amorphous carbon layer (ACL) such as advanced patterning film (APF) is generally selected as one possible hard mask material for variety of dielectric etching application beyond 65 nm technology nodes to improve the etch process margin from reduction of resist thickness. Most of the APF etching application for DRAM, flash and logic technology are done typically on 1 µm film thickness to enable specific integration scheme of nanotechnology. The challenges of etching high aspect ratio ACL features are bowing prevention during etching, hard mask selectivity and the etch rate improvement for throughput concern. In this paper, high aspect ratio (HAR) contact through ACL layer is developed by soft etching capability using high frequency source plasma etch chamber. This development work was done in the dielectric etch chamber consisting of the superimposed dual bias power and a capacitive coupled source power > 100 MHz, which can be operated in either low density process regime for higher resist selectivity, or in high density process regime for profile control, resist integrity, minimal striations and effective chamber cleaning. With high frequency source power, fast etch rate >6000 Å/min of ACL has achieved with minimum hard mask corner chopping from small plasma self bias. All the process trends are characterized with profile control, hard mask selectivity and etch rate.

11:20am **PS1+MS+NM-TuM11 Chamber and Process Development of High Aspect Ratio Deep Trench Si Etch for DRAM Application below 60 nm**, *S. Barth, A. Henke,* Qimonda, Dresden, Germany*; A. Kersch,* Qimonda, Munich, Germany*; M. Reinicke,* University of Technology, Germany*; W. Sabisch,* Qimonda, Munich, Germany*; J. Sobe, A. Steinbach,* ***S. Wege,*** Qimonda, Dresden, Germany

For Qimonda's DRAM Technology the deep trench etched into silicon is the base for the capacitor concept. The shrink of lateral dimensions at approximately constant capacity specifications leads to increased deep trench aspect ratio requirements. Therefore high selectivity to the etch mask and excellent uniformity is needed, especially for technologies below 60nm. In this paper we describe the development of a new DT plasma etch chamber and process to fulfill these requirements. Simulations (an equivalence circuit plasma model and surface reaction models) were combined with in-situ plasma measurement techniques (QMS, high resolution OES, IR absorption spectroscopy, SEERS and Langmuir probe sensor wafers) and technological experiments, to characterize hardware features and process conditions. To achieve high Si etch rate and selectivity, plasma density and electron energy distribution in the plasma bulk, and ion energy distribution on the wafer surface can be optimized through multi frequency cathode excitation. The selectivity is further enhanced by using advanced hard mask materials and combining of etching and deposition process regimes. Excellent uniformity has been achieved by new tool components, e.g., multi zone gas distribution and wafer temperature control. In addition, the etch process chamber includes new features for process control, in-situ wafer surface temperature and trench dept measurement. The equipment and process development was accomplished through close cooperation between Qimonda and the tool supplier.

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