Plasma Science and Technology
Room 2009 - Session PS-MoA

Manufacturing and Scientific Challenges for Plasma Processing at 32 nm

Moderator: S. Shankar, Intel

2:00pm **PS-MoA1 Core Technologies for The Transition from Si Technology to Nano-technology**, ***H. Watanabe***, Semiconductor Leading Edge Technologies, Inc. (Selete), Japan **INVITED**

Selete grapples with development of hp45/32nm module technology based on the results of Selete and MIRAI until now with promoting the variety project to meet widely the request which diversify. We take part in a new national project (MIRAI3) to develop the leading edge technologies of EUV lithography, post Cu interconnect, and robust transistor, and demonstrate the presence of Selete by worldwide preceding. In this presentation, I will introduce the challenge of Selete for 32nm module technologies and also discuss core technologies for the transisition from Si technology to Nano-technologies.

2:40pm **PS-MoA3 Patterning Technology for Sub-50 nm Memory Devices**, ***C.-J. Kang***, SAMSUNG Electronics, Korea **INVITED**

In the era of sub-50 nm memory devices, patterning technology encounters many challenges, which arise from the introduction of immersion ArF lithography with high numerical aperture, a complex device structure, and the use of new materials. First of all, in the immersion technology, 100 nm thickness of ultra-thin resist process is used and it is likely to generate particles to cause defects. In addition, the reduction of a line width roughness (LWR) and overlay error between layers are getting more difficult. Second, in the plasma etching technology, the advanced features such as 3 dimensional FinFET structure force to develop a highly selective etching process. Finally, the introduction of new materials such as High-k dielectric, metal gate, and phase change materials are more challenging in the view point of profile and selectivity. Since the process window is getting narrow, control and monitoring technologies such as advanced process control (APC) and advanced equipment control (AEC) are strongly required. For the development and manufacturing of sub 50-nm memory devices, the patterning technologies should overcome many difficulties, which is related to not only the lithography and etching process itself, but also hardware development.

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